

NORTHWESTERN UNIVERSITY TECHNOLOGICAL INSTITUTE

ECE 270

Experiment #8
DIGITAL CIRCUITS
Prelab

1. Draw the truth table for the S-R Flip-Flop as shown in the textbook. Draw the truth table for Figure 7.
2. Show the truth table, Boolean expression and schematic for a half-adder with carry.
3. Show the truth table, Boolean expression and schematic for an equality comparator.
4. Show the Boolean expression and schematic for a 2-to-1 multiplexer.

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ECE 270

Experiment #8 **DIGITAL CIRCUITS - Part I**

Reference: Smith, R.J., Electronics, Circuits and Devices, Wiley, 1980. Chapters 7 & 8.

In a large-scale digital system, such as a computer, there are only a few basic operations which must be performed. These operations may be repeated many times. The four circuits most commonly used in digital systems are the AND, OR, NOT and FLIP-FLOP. These circuits are called logic gates. A gate is a device that controls the flow of data, which is usually made up of a series of pulses.

A digital system functions in a binary manner. In other words the system uses devices which operate in only two possible states. The most common designation for these states are 0 and 1. Binary arithmetic is usually carried out using these symbols. A binary digit is referred to as a bit.

To help us understand and use logic circuits, we use symbols to represent the various logic operations. We define the function of the logic operation in a truth table, which shows all possible input combinations and the outputs resulting from them.

The OR gate

The OR gate has two or more inputs and a single output. It operates on this definition: The output of an OR assumes the 1 state if one or more inputs assume the 1 state (See Figure 1). Each input can take on either the 0 or 1 state (perhaps representing 0.0V and 5.0V respectively). Instead of defining the operation of the OR gate in words, we can either use a truth table, or write out an equation specifying the output.

The AND gate

The AND gate has two or more inputs and a single output and its definition is: The output of an AND assumes the 1 state if and only if all the inputs to the gate take on the 1 state. The truth table and symbol for the AND gate is in Figure 2. Notice that a "dot" (multiplication symbol) is placed between the two inputs to show the AND operation.

The NOT gate

The NOT gate has one input and one output and its function is to yield an output state which is the complement of the input state. That is, if the input is a 1, the output will be a 0 and vice versa (See Figure 3).

The NOR gate

The NOR gate has two or more inputs and a single output. It has a similar operation to an OR gate except it takes the complement of the output. The name NOR is from NOT-OR. So the output of the NOR gate is NOT A OR B (See Figure 4).

The NAND gate

The NAND gate also has two or more inputs and a single output. It also takes the complement of the output. The output is NOT-AND or NOT A AND B.

PROCEDURE

The purpose of this experiment is two fold. One purpose is to familiarize you with the various functions of the IPC Digital Trainer, the other is to introduce you to the process of wiring digital circuits using actual integrated circuits and their corresponding data sheets.

The IPC Digital Trainer has a self-contained 5 volt DC power supply. All integrated circuits (IC's) in this experiment will operate on a V_{CC} of 5 volts. The Trainer also has switches to provide logic 0's and 1's, momentary contact switches to provide pulses manually, a 555 timer IC which is used as a clock (similar to a square-wave generator except that there are only two frequencies available, LO and HI, which are varied through the use of a switch) and various display devices used to monitor the inputs and outputs of an IC. These devices are light emitting diodes, or LED's. They are used in digital circuits because of their low current drain on an IC, usually on the order of 15mA.

For this experiment, all IC chips are placed across the center channel of the board with the small indentation of the chip placed on the left. To identify the pins on an IC, place the indentation on the left and view the IC from the top. Pin 1 is in the lower left corner. The pins are numbered consecutively in a counterclockwise direction (See Figure 6).

I. Truth Tables

Obtain the truth tables for the following gates:

SN74LS00 - Quadruple 2-input NAND gate

SN74LS04 - Hex Inverter

SN74LS08 - Quadruple (Quad) 2-input AND gate

SN74LS32 - Quad 2-input OR gate

Note: Make sure that V_{CC} and Ground are connected to the IC and use the data sheets provided to obtain pin numbers for input and output. Attach an LED to the output pin to monitor whether the output of a specific gate is a 0 or a 1. Use level switches to provide the inputs to the gate.

1. From measured results draw the truth tables for the above gates.
2. Do they agree with the definitions of the gates?

II. Logic Circuit Analysis

Boolean algebra allows us to manipulate logic statements directly without using truth tables. We can also use Boolean algebra to simplify complex circuits, which allows us to use fewer parts. The analysis of a logic circuit is straightforward. First, trace through the circuit and write down the function occurring at the output of each gate. The final expression for the output can then be simplified using Boolean algebra. Refer to Chapter 8 in Electronics for specific examples.

III. Logic Circuit Synthesis

To obtain various logic operations, the logic designer starts with a truth table, and proceeds to convert the truth table into a convenient form, and then uses standard logic elements to realize the operation.

3. Design a half-adder. First draw a truth table and then obtain expressions for the sum and carry outputs of the adder. Then build the circuit and verify that this logic circuit realizes the sum of two binary digits.
4. Design an equality comparator. This is a device that yields an output of 1 only if inputs A and B are equal. Use the same procedure in 3 above.

Note: Use an LED to monitor the output and use the level switches as your inputs into the circuit.

IV. Registers

We have seen how logic circuits are used to process binary data. In addition, large-scale digital systems must also contain memory devices to store either data or results. A device that stores a bit of data must have two distinct states, a 0 or a 1. It must remain in that state until instructed to change. This device is called a flip-flop. It is used as one of the basic memory elements in all digital systems. A flip-flop is constructed out of either NAND or NOR gates (See Figure 7).

5. Show that the device in Figure 7 is a memory element by using a truth table to verify $S, R, Q, \overline{Q}$.
6. Construct the flip-flop of Figure 7 and apply inputs to S, R through level switches and monitor Q and $\overline{Q}$ with LED's.
7. Does your circuit agree with the truth table? Is there an unstable state? Why?

V. J-K Flip-Flop

In addition to the R-S flip-flop, there are other types of flip-flops that avoid the ambiguity that was observed with the R-S flip-flop. In other words, we don't have the outputs $Q, \overline{Q}$ equal to the same value, which in terms of logic circuit identities is incorrect. In this experiment, we will use a J-K flip-flop. It is a very useful memory element, because it has three different modes of response (See Figure 8).

With unequal inputs, the J-K flip-flop operates in the same manner as an R-S flip-flop. Remember that the J-K flip-flop has a clock input which controls when it changes output states. It will not change states unless there is a clock pulse, regardless of what the inputs to J and K are.

For J set to 1 and K set to 0, the clock SETS the output Q to 1. When K is 1 and J is 0, the clock RESETS the output Q to 0. With both J and K set to 1, the output toggles between 0 and 1 each time there is a clock pulse. This configuration is called the T flip-flop.

Obtain a SN74LS76 Dual J-K flip-flop with PRESET and CLEAR. Mount the IC in the IPC Digital Trainer. Use the data sheets supplied to obtain the pin configurations for inputs and outputs.

8. Verify the truth table given in Figure 1 and record your results.

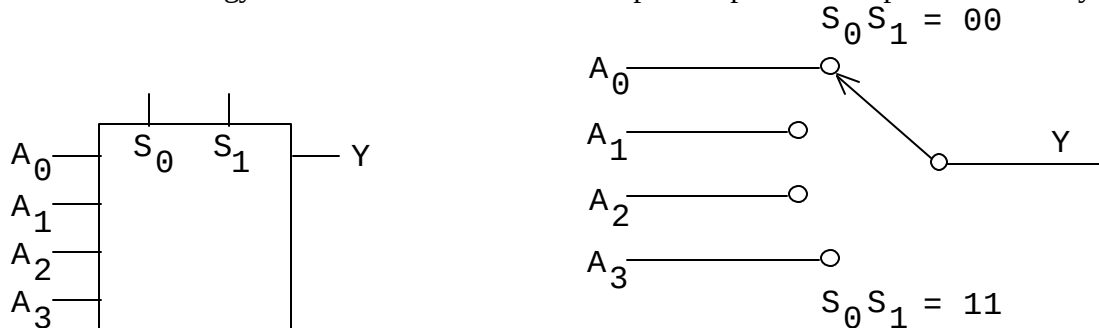
Note: Use level switches for the J and K inputs and use the pulse switches for the clock. Monitor $Q, \overline{Q}$ with LED's.

Connect one of the pulse switches to the PRESET input of the flip-flop. Apply a pulse and observe the output LED's. Then reconnect the switch to the CLEAR input. Apply a pulse and observe what happens.

9. What are the functions of the PRESET and CLEAR inputs?
10. Why do you think that these inputs were placed on the IC?

VI. Multiplexer

A multiplexer is a device which gates one out of 2^n inputs to a single output. If $n = 2$, we have a 4-to-1 multiplexer. A mechanical analogy is used to describe how a multiplexer operates. The pointer is a rotary switch.



If S_1 & $S_0 = 0$, then $Y = A_0$.

If $S_1 = 0$ and $S_0 = 1$, then $Y = A_1$.

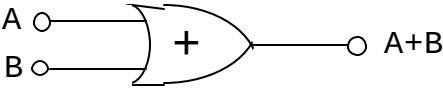
If $S_1 = 1$ and $S_0 = 0$, then $Y = A_2$.

If S_1 & $S_0 = 1$, then $Y = A_3$.

S_1 & S_0 specify which input gets connected to the output. The multiplexer that you will develop in the lab will perform the same function. Only it will be done electronically instead of mechanically.

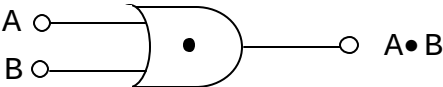
11. Design a 2-to-1 multiplexer. The truth table is given below. Determine the corresponding Boolean expression and logic diagram.
12. Build and test the circuit, recording your results.

S_0	A_1	A_0	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1



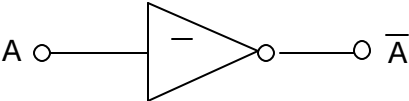
A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

Figure 1



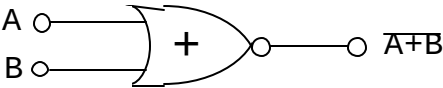
A	B	A•B
0	0	0
0	1	0
1	0	0
1	1	1

Figure 2



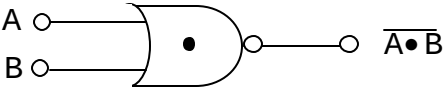
A	$\overline{A}$
0	1
1	0

Figure 3



A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

Figure 4



A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

Figure 5

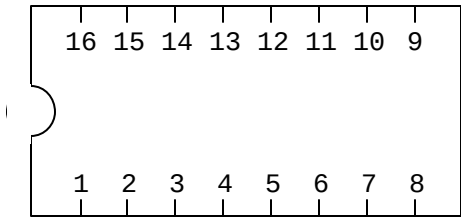


Figure 6

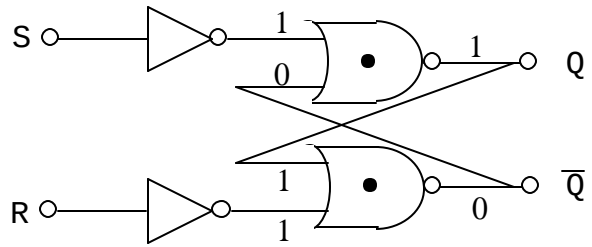


Figure 7

J	K	Q
0	0	Q_0
0	1	0
1	0	1
1	1	$\overline{Q_0}$

Figure 8

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ECE 270

Experiment #8 DIGITAL CIRCUITS - Part II

In the previous experiment we saw how some basic logic gates (e.g. OR, AND, etc.) could be combined to produce slightly more complex logic functions (e.g. XOR, multiplexer). This experiment will demonstrate that complex functions can be integrated on to a single chip. By putting these devices on a single chip, the equipment that uses them will use less power and require less space.

Counters

Flip-flops can be connected together to function as counters which can be used to keep track of events occurring in digital computers or in specialized instrumentation. Refer to Chapter 8 in Electronics for specific details on various types of counters.

Integrated circuit manufacturers often combine many flip-flops into one IC to serve as a counter. In this part of the experiment, we will examine the 74LS192 Presettable Decade Counter. It is designed to count from 0 to 9 and then start all over again from 0. It can either count up or down, depending on how the clock is connected to it. The output of the counter Q_D Q_C Q_B Q_A is in binary coded decimal (BCD) form (See Figure 1). By connecting this device to a BCD-to-seven-segment decoder, we can obtain a visual display of the output of the counter. This is the same method used in electronic calculators. The data comes out in BCD form and the decoder changes it into a form that can be displayed on LED readout.

Q_D	Q_C	Q_B	Q_A	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

Figure 1

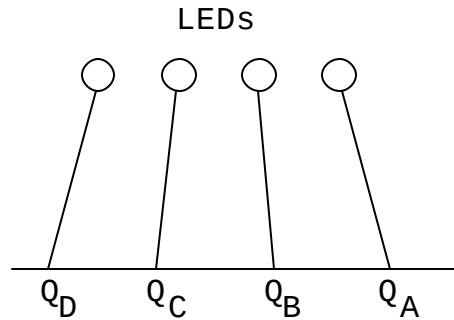


Figure 2

Procedure

Using the data sheet provided, connect the 74LS192 as a count UP decade counter. Be sure that you read the data sheet carefully because certain pins have to be either connected to V_{CC} or Ground for proper operation. First, connect power to the IC. Then connect the outputs Q_D Q_C Q_B Q_A to the LED indicators (See Figure 2). Then connect the clock to the count UP pin.

1. Does the IC count from 0 to 9? Record each count display of the LED's and convert the binary digit to a decimal digit.

In order to see that this device can be preset to a particular number, use the level switches as inputs to the DATA D, DATA C, DATA B and DATA A inputs on the IC. Use a pulse switch to LOAD the data into the counter.

2. What level does the LOAD pin have to be in order to load the data into the IC?

To see how the BCD-to-seven-segment decoder works, connect the Q outputs to A3, A2, A1 and A0 inputs of the decoder and observe the LED 7-segment display.

3. Does it display the actual binary input (tabulate your results)?

Set up the configuration to make the 74LS192 count DOWN. Read the data sheet for procedures.

4. Describe what happens.

Use the level switches to load a binary number greater than 9 into the counter.

5. What happens when a binary number greater than 9 is loaded into the 74LS192 counter?

Information Processing

In a large-scale digital system, there are usually many sources of information and many destinations. In order to save money, space, and wires, digital information is usually sent on a common "bus". There are devices used to route the information onto specific paths. In this experiment, we will look at two widely used devices: The decoder/demultiplexer and the data selector/multiplexer.

The decoder/demultiplexer has one input line and many output lines. The IC we are going to use is the 74LS154 4-line to 16-line decoder/demultiplexer. It allows decoding of a 4bit binary coded input into one of 16 separate outputs.

The data selector/multiplexer has many input lines and only one output line. It chooses the one source whose address is on the select terminals. In our experiment, we will use the 74LS153 dual 4-to-1 multiplexer. It contains two 4-to-1 multiplexers. See the accompanying data sheets for information.

Procedure

Connect the power supply to the 74LS153 dual 4-to-1 line multiplexer. Connect the strobe inputs 1G and 2G to Ground (GND). Use two level switches to address the input line that is desired. For example, apply the clock to input 2C2. To address that line, B has to be set to 1 and A has to be set to 0 (See truth table on data sheet). Notice that the clock is at the output 2Y. Use the LEDs to monitor the inputs and the outputs.

6. Tabulate a truth table for this IC.

A multiplexer can be used for combinational logic circuit design. If we are working with a 4-to-1 multiplexer, there are 4 input lines, 2 select lines, and 1 output. This multiplexer can be connected to a circuit in such a way that it acts as a 2 input (which equals the number of select lines) single output logic circuit.

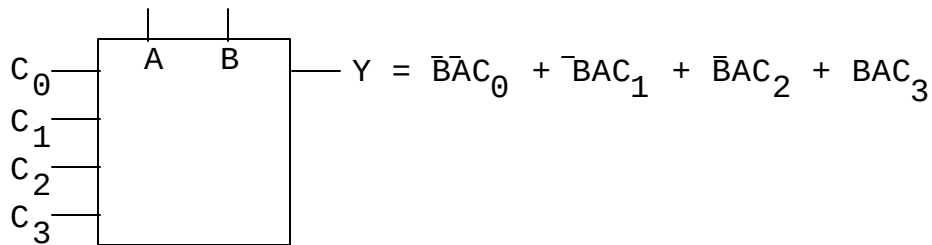


Figure 3

Figure 3 gives the expression for the output of a 4-to-1 multiplexer. If you compare it to the truth table for the 74LS153 you can see that this is a correct description of the multiplexer output.

What if we constrain C_0 and C_2 to be 0 all the time? Then the first and third terms of Y in Figure 3 are zero and the output reduces to $Y = \bar{B}AC_1 + BAC_3$. Now, what if we further constrain C_1 and C_3 to equal 1. Then $\bar{B}AC_1 = \bar{B}A$ and $BAC_3 = BA$. The expression for Y reduces to: $Y = \bar{B}A + BA$

The truth table for this expression is given Figure 4.

B	A	Y
0	0	0
0	1	1
1	0	0
1	1	1

Figure 4

To wire the multiplexer to perform this function we would simply connect C_0 and C_2 to GND and C_1 and C_3 to +5V. The result is a 2 input single output combinational circuit.

The above example is overly simple (since $Y = A$), but consider a 4 input single output system. Logic functions for 4 inputs could result in very complex truth tables that would require many chips to realize in hardware. One 16-to-1 multiplexer could be used to realize these same functions.

7. In Figure 5 is a truth table for a 2-input single output function. Determine an expression for Y in terms of A, $\bar{A}$, B, $\bar{B}$ similar to the one given in the example. It should be an expression that OR's 2 or more terms of the form $\bar{A} \bar{B}$, $A\bar{B}$, etc. Having determined this expression, determine which inputs to the multiplexer should be grounded and which ones connected to +5V.

B	A	Y
0	0	1
0	1	1
1	0	0
1	1	1

Figure 5

8. Wire the circuit as determined above. Connect A and B to 2 level switches. Verify that the circuit produces the desired output.
9. Explain why it would be desirable to implement a function in this manner instead of using several logic gates.

Remove the 74LS153 and replace it with the 74LS154 4-line to 16-line decoder/demultiplexer. Notice that this chip has 24 pins on it. The mounting procedure is the same as the other chips. Apply V_{CC} and GND in the normal way.

Apply a clock input to G1 and tie G2 to GND. Use the 4 level switches on the trainer as inputs to D, C, B and A. By changing the address, the clock input will appear at one of the 16 outputs. Look at the truth table supplied on the data sheet and see how this is accomplished.

10. Verify the truth table.
11. What are some of the uses of decoders, demultiplexers, multiplexers and data selectors?