

NORTHWESTERN UNIVERSITY TECHNOLOGICAL INSTITUTE

ECE 270

Experiment #6
FIELD EFFECT TRANSISTORS
Prelab

1. Perform part 4 of the Procedure.

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INTRODUCTION

A field-effect transistor (FET) is a three terminal device which can be modeled as a voltage controlled current source. From an operating viewpoint, the major difference between the FET and a bipolar junction transistor (BJT) lies in the fact that its input impedance is so high that under normal conditions, input currents will be negligible. This has the side benefit of simplifying bias network design.

We will be using an N-channel, depletion type, junction field effect transistor (JFET) in this experiment. Its three terminals are known as the Gate, Source and Drain. The Gate (G) lead is the control element, while the Source (S) and Drain (D) leads are attached to opposite ends of a "channel" of (in this case) N-type silicon material. The Source lead is usually connected to the end of the channel which is physically nearest the Gate structure, but since most American-made JFETs feature symmetrical gate construction, the Source and Drain leads may often be interchanged in a circuit with no important observable differences.

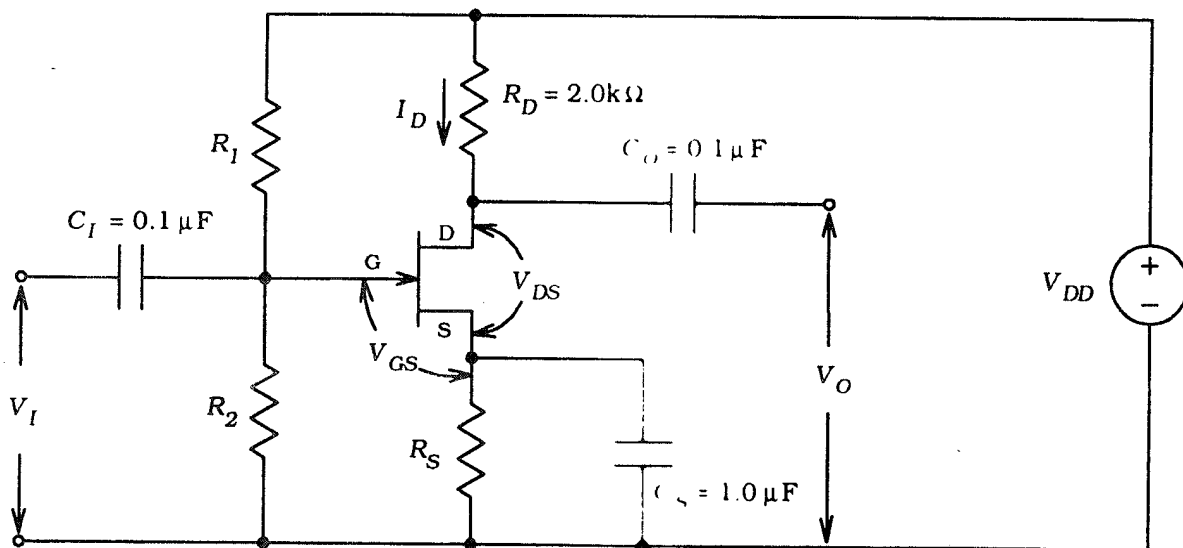
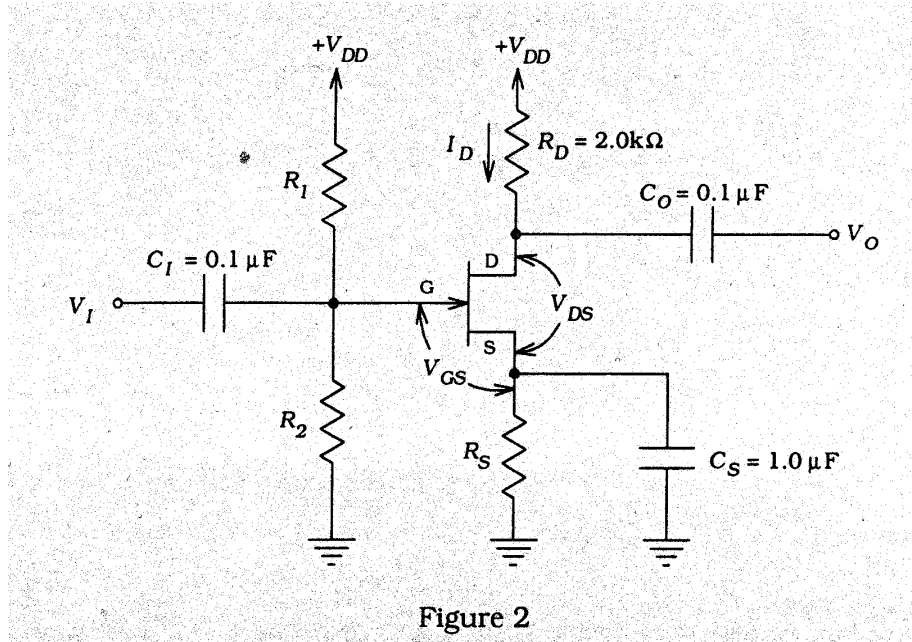


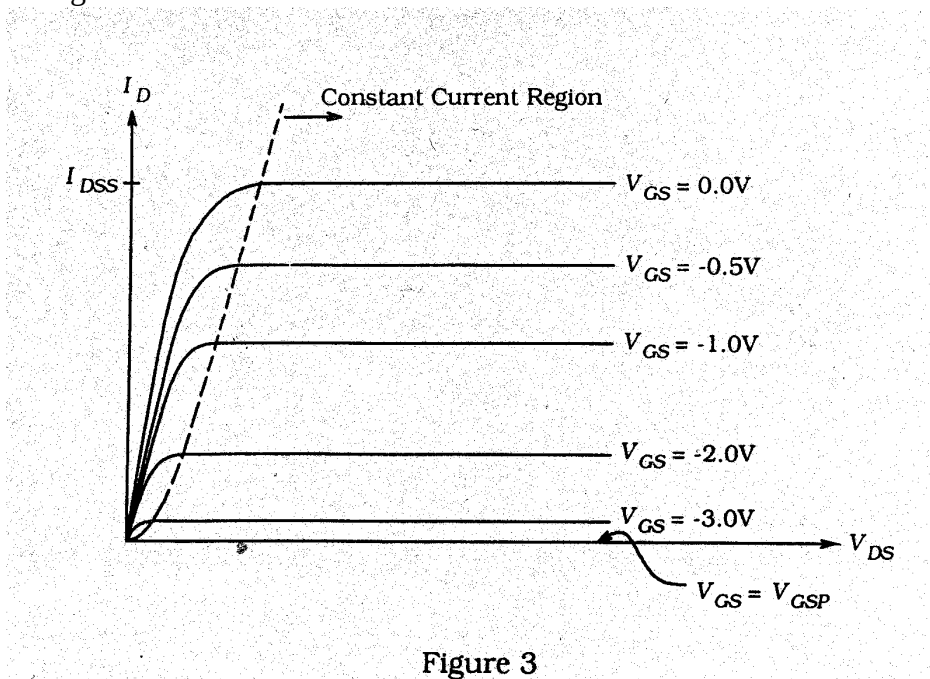
Figure 1

The Gate, Source and Drain leads may be thought of as corresponding roughly to the Base, Emitter and Collector leads of a bipolar transistor. Of course, a JFET may be connected into a circuit in any of the three configurations discussed in the textbook, but we will use the common source arrangement as shown in Figure 1. To reduce the number of wires shown in the circuit, a symbol is often used to represent a common point of connection (usually the circuit ground or common). In very complicated circuits, this can help to reduce the confusion of trying to trace down many lines on the schematic. Figure 2 is the same circuit as shown in Figure 1, but uses this symbol for the circuit ground.

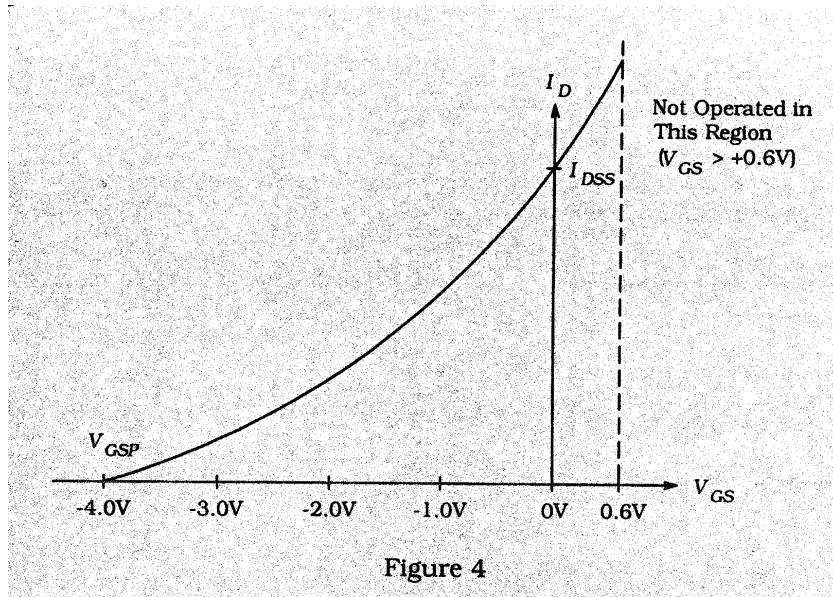


Also, note that this schematic doesn't show V_{DD} , but simply points to the positive terminal of V_{DD} . It is understood that V_{DD} 's common (black terminal on the power supply) is connected to the circuit ground. The input signal is connected between V_I and circuit ground the output voltage (V_O) is measured with respect to circuit ground also.

Because of the high input impedance, we normally do not plot the common source "input characteristics" since all we would expect to see is a straight line at $I_G = 0$. However, we are interested in the "output characteristics" of which a typical set is shown in Figure 3.



We may also pick a value for V_{DS} in the "constant current" region where I_D is nearly independent of V_{DS} and plot the "transfer characteristics" which appear in Figure 4.



In order to bias a FET circuit, we can simply pick our operating point (I_{DQ} and V_{DSQ}) and read off the desired value of V_{GS} from the curve tracer (experimentally). It is also possible to calculate the value of V_{GSQ} once we have measured two important parameters. A few preliminary definitions are in order:

$$I_{DSS} = I_D \Big|_{V_{GS}=0, V_{DS}=-V_P}$$

This is the *saturated drain to source current*. It is the drain current when $V_{GS} = 0$ and $V_{DS} = -V_P$ (this is at the constant current line).

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \Big|_{V_{DS}}$$

This is called the transistor's transconductance, and is calculated as current over voltage which is one over resistance or conductance. V_{GS} is the input while I_D is proportional to the output. Therefore, it is the transfer (output to input) conductance (transconductance). Using a small AC gate to source voltage ($\ll |V_P|$), g_m is defined as the resulting small signal AC drain current over the small signal AC gate to source voltage. It is measured at the operating point (Q point) and corresponds to the slope of the curve in Figure 4 at the Q point.

$$g_{mo} = \frac{\Delta I_{DS}}{\Delta V_{GS}} \Big|_{V_{GS}=0}$$

This is the maximum transconductance of the transistor and corresponds to the slope of the curve in Figure 4 where the curve crosses the $V_{GS} = 0$ axis (y-axis).

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} \Big|_{V_{GS}}$$

This is the "dynamic drain resistance" and is measured at the Q point. Because this value is usually quite large ($>10\text{k}\Omega$), the lines in Figure 3 are drawn as being horizontal (in the constant current region). In reality, these lines have a finite slope which is $1/r_d$.

Some useful relationships include:

$$V_{GSP} = \frac{-2I_{DSS}}{g_{mo}}$$

$$V_{GSQ} = \left(\frac{2I_{DSS}}{g_m} \right) \left(\sqrt{\frac{I_{DSQ}}{I_{DSS}}} - 1 \right)$$

As can be seen from the above equations, once I_{DSS} and g_m have been measured, V_{GSQ} can be calculated. You will note that V_{GS} has a negative polarity for an N-channel JFET, while V_{DS} is positive. In order to avoid the necessity of using two power supplies, a source resistor (R_S) is used. If the gate bias network is properly chosen, this creates a positive voltage drop across R_S which places the source at a higher potential than the gate. Thereby, creating a negative value for V_{GS} .

Notice also that since the gate current is negligible, the source current and drain current are identical. In addition, the values of R_1 and R_2 can be chosen independently of the gate current.

In this experiment, you are to design for $V_{DSQ} = 10\text{V}$, $V_{DD} = 18\text{V}$, $I_{DQ} = I_{SQ} = I_{DSQ} = 2.5\text{mA}$.

PROCEDURE

1. Ask the TA to measure I_{DSS} , g_m , g_{mo} and r_d on the curve tracer. Also, estimate V_{GSP} . Record these values for your write-up.
2. Ask the TA to measure V_{GSQ} for the operating point on the curve tracer. Calculate V_{GSQ} from the equations given earlier and compare the two values.
3. Calculate V_{GSP} (pinch-off) and compare to your measurement.
4. Write a loop equation (DC) for the output circuit, and find the value of V_S (Source to **Ground** voltage) and calculate R_S .
5. From your calculated value of V_S and the calculated value for V_{GSQ} , find the voltage you need across R_2 .
6. Remembering that $I_G = 0$, choose R_1 and R_2 in the right ratio to give the desired voltage across R_2 (Gate to **Ground** voltage). Make the sum of R_1 and R_2 greater than $100\text{k}\Omega$.
7. Obtain all of the circuit components for Figure 1 and assemble the circuit. Tabulate measured values of V_G (the Gate to **Ground** voltage or the voltage across R_2), V_S (the Source to **Ground** voltage or the voltage across R_S) and V_D (the Drain to **Ground** voltage). Include in this table the calculated values for each measurement and the %Error (assuming calculated values correct - of course).

In order to see how this circuit should behave as an amplifier of AC signals, we need to consider the small-signal model for the transistor as shown in Figure 5. For AC signals, the input impedance of the FET looks like an open circuit ($R_{IN} = \infty$) and the output provides an amplified version of the input signal (represented here by a current source on the output which is controlled by the input voltage). The output of the FET does have some output resistance (r_d) which is large.

Now, replacing the transistor in Figure 1 with this model and replacing all capacitors with short circuits (capacitors act like short circuits at high frequencies) and replacing the DC power supply (V_{DD}) with a short circuit (superposition principle), Figure 1 is transformed into Figure 6 which is an appropriate circuit for the AC analysis.

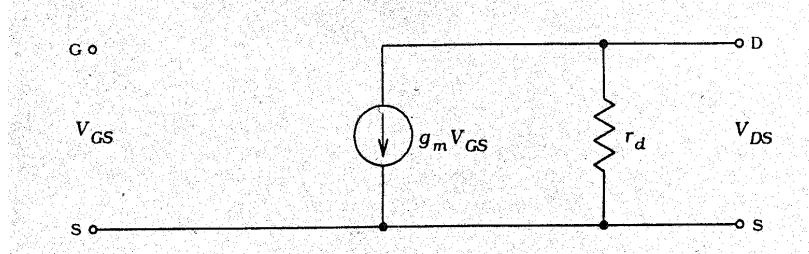


Figure 5

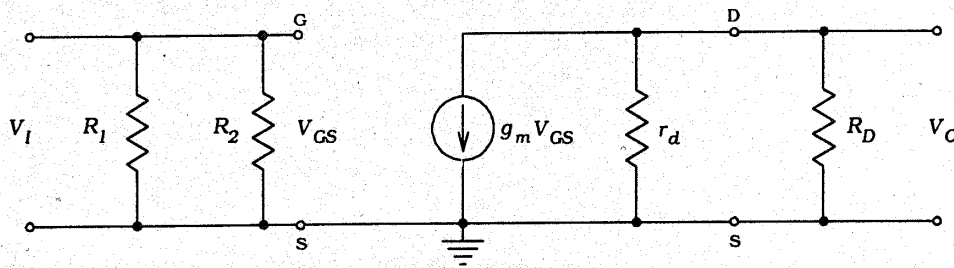


Figure 6

Elementary network analysis will show that the following relations hold:

$$\text{Input resistance} = R_1 || R_2 = R_1 R_2 / (R_1 + R_2)$$

$$\text{Output resistance} = r_d || R_D = r_d R_D / (r_d + R_D)$$

$$A_v = V_{OUT} / V_{IN} = g_m (r_d || R_D) = g_m r_d R_D / (r_d + R_D)$$

8. Calculate the input resistance, output resistance and voltage gain for your circuit.
9. Apply a 2kHz signal to your amplifier and measure the above parameters. Compare theoretical and experimental results (tabulate as usual). To measure the input resistance, measure the magnitude of the input signal before and after applying it to the circuit. Recalling that the function generator has an output resistance of 50Ω , you have a simple voltage divider between 50Ω and your amplifier's input resistance. If your input resistance is large, you may have to add a large resistor ($1k\Omega$ to $10k\Omega$) in series with the source resistance in order to see any drop in voltage when the source is applied to the circuit. Similarly, measure the output of your amplifier with and without a load resistance to calculate the output resistance. These added resistances used to measure the input and output resistance of your amplifier should be measured to obtain accurate results.