PRITH BANERJEE

Walter P. Murphy Professor and Chairman
Department of Electrical and Computer Engineering
Director, Center for Parallel and Distributed Computing
Northwestern University

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Residence:
2130 Chandler Lane
Glenview, Illinois 60025
(847) 657-8749

PERSONAL: Born July 17, 1960, U.S. citizen, married, one son.

EDUCATION:

- Ph.D. (Dec. 1984), Electrical Engineering, University of Illinois, Urbana
- M.S. (Dec. 1982), Electrical Engineering, University of Illinois, Urbana
- B.Tech. (Jun. 1981), Electronics and Electrical Eng., Indian Institute of Technology, Kharagpur

WORK EXPERIENCE:

- Aug. 2004-present, University of Illinois at Chicago, Dean, College of Engineering. Responsible for six academic departments, 120 faculty, 1800 undergraduates, 1000 graduate students.

- 1998 - 2001, and 2002-2004, Northwestern University, Chairman and Professor, Electrical and Computer Engineering. Responsible for a department with 31 faculty, 120 graduate students, 250 undergraduate students; Instrumental in developing some novel undergraduate curriculum revisions, strong industrial interactions, and collaborative research funding.

- 1996 - present, Northwestern University, Director, Center for Parallel and Distributed Computing. Responsible for building a center with 12 faculty, being a principal investigator of five large research projects with more than $8 million in funding from DARPA, NSF, NASA, DOE, and others.

- July 2002 – June 2004, AccelChip, Inc, Founder and Chief Scientist. Responsible for providing technical leadership for the company.

- July 2000 - June 2002, AccelChip, Inc., Founder, President and CEO. Responsible for founding the company, raising $2.3 million in Venture Capital funding, hiring a top management team, growing the company to about 25 employees, developing the first product AccelFPGA, and generating more than $800,000 in revenue.

- 1994-1996, University of Illinois, Director, Computational Science and Engineering. Responsible for building a CSE graduate program in 10 engineering departments setting up a CSE lab, and coordinating the writing of several large research proposals.

- 1993-1996, University of Illinois, Professor, Electrical and Computer Eng, Professor, Coordinated Science Laboratory. Supervised more than 25 Ph.D. and 20 M.S. students, and had four large research projects.

- 1989-1993, University of Illinois, Associate Professor, Electrical and Computer Engg. Research Associate Professor, Coordinated Science Laboratory.

- 1985-1989, University of Illinois, Assistant Professor.

AWARDS AND HONORS:

- Received the Taylor Booth Award for Outstanding Educator in the field of Computer Science and Engineering, awarded by the IEEE Computer Society, 2001.

- Elected Fellow of Association of Computing Machinery (ACM), 2000

- Awarded the Best Paper Award at the Int. Symp. on Parallel and Dist. Systems, Cancun, MX, May 2000.

- Awarded the Best Paper Award at the IEEE VLSI Test Symposium, Monterey, CA, April 1998.

- Recipient of the 1996 Frederick Emmons Terman Award from the ASEE's Electrical Engineering Division, sponsored by Hewlett-Packard Company, presented to an Outstanding Young Electrical Engineering Educator, for publishing the textbook "Parallel Algorithms for VLSI CAD".

- Elected Fellow of Institution of Electronics and Electrical Engineers (IEEE), 1995

- Awarded the 1994 Outstanding Paper Award from the International Conference on Parallel Processing, St. Charles, IL, August 1994.

- Awarded the 1992 University Scholar Award from the University of Illinois.

- Recipient of the 1992 Senior Xerox Award for Faculty Research, University of Illinois.

- Awarded the National Science Foundation's Presidential Young Investigator Award 1987.

- Awarded the IBM Young Faculty Development award for research in Computer Engineering, 1986.

- Recipient of the IBM Graduate Fellowship in Computer Science, 1983 and 1984.

- Awarded the President of India Gold Medal for highest rank among all disciplines the Indian Institute of Technology, Kharagpur, 1981.

REPORTED IN THE NEWS:

- University of Illinois at Chicago News Release, Thursday June 3, 2004

http://tigger.uic.edu/htbin/cgiwrap/bin/newsbureau/cgi-bin/index.cgi?from=Releases&to=Release&id=813&frommain=1

- Chicago Sun Times, Friday June 4, 2004

http://www.suntimes.com/output/news/cst-nws-dean04.html

- Hindustan Times, Saturday June 5, 2004

http://www.hindustantimes.com/news/5967_805523,00160006.htm

- Reported in May 2003 EE Times

http://www.eedesign.com/news/OEG20030507S0036

- Reported in June 2002 Electronic Design Article on AccelChip,

http://www.e-insite.net/electronicnews/index.asp?layout=article&articleId=CA223041%20

- Reported in Apr. 2002 Electronic News Article on AccelChip, http://www.e-insite.net/electronicnews/index.asp?layout=article&articleId=CA209256

- Reported in Apr. 2002 EE Times Article on AccelChip, http://www.eedesign.com/story/OEG20020402S0049

- Reported in Aug. 2000 EE Times Article on MATCH Compiler, http://www.eet.com/story/OEG20000810S0021

- Reported in Aug. 2000 EE Times Article on PACT Compiler, http://www.eet.com/story/OEG20000817S0008

RESEARCH CONTRACTS AND GRANTS:

- National Science Foundation (Principal Investigator), "High Level Synthesis of Low-Power Embedded Systems," $300,000, 2004-07, Submitted Dec. 2003.
- National Science Foundation (Principal Investigator), "Automated Translation of Software Binaries onto Embedded Systems-on-a-Chip," $300,000, 2004-07, Submitted Dec. 2003.
- National Science Foundation (Principal Investigator), "Improving Compilation Techniques for Application Specific Hardware Using Runtime Information," $700,000, 2004-07, Submitted Nov. 2003.
- National Aeronautics and Space Administration (NASA) (Principal Investigator), "MATLAB Based Adaptive Computing for NASA Image Processing Applications," $309,835, 2000-03.
- Defense Advanced Research Projects Administration (DARPA) (Principal Investigator), "PACT: Power Aware Architectural and Compilation Techniques," $1,202,906, 2000-2003.
- Synplicity Corporation (Principal Investigator), "Software Tools for FPGA and ASIC Synthesis and Verification," 2003, software donation.
- Synopsys Corporation (Principal Investigator), "Software Tools for Logic Synthesis," 2000-2002, software donation, (obtained through University Program)
- Cadence Design Systems (Principal Investigator), "Tools for Electronic Design Automation," 2000-2002, software donation, (obtained through University Program)
- Microsoft Corporation (Principal Investigator). "New Initiatives in the Electrical and Computer Engineering Department," 2000-2001, hardware, software and cash donation, $690,000.
- Motorola Foundation (Principal Investigator), "New Initiatives in the Electrical and Computer Engineering Department," 1999-2004, cash donation, $500,000.
- Defense Advanced Research Projects Administration (DARPA) (Principal Investigator), "A MATLAB Compilation Environment for Adaptive Computing Systems," $1,855,662, 1998-2001.
- Department of Energy, ASCI Level-2 (Co-Principal Investigator), "Large High-Performance Data Management, Access, and Storage Techniques for Tera-Scale Scientific Applications," $876,000, 1998-2001.
- Defense Advanced Research Projects Administration (DARPA) (Co-Principal Investigator) "Architectures, Compilers, and Configuration Management of Reconfigurable Computing for Mass-Market Computing," $1,981,349, 1997-2000.
- National Science Foundation (Principal Investigator), "A High-Speed Distributed Computing Infrastructure", $906,512, 1997-2002.
- National Science Foundation (Principal Investigator), "Efficient Compilation Issues in Distributed Memory Multicomputers," $94,000, 1996-99.
- Mentor Graphics Corporation (Principal Investigator), "VLSI Computer Aided Design Tools", 1996-02,software donation.
- IBM Corporation (Principal Investigator), "IBM Research Partnership Award: Parallelizing Compiler for Distributed Memory Multicomputers", $40,000, 1995-96.
- Defense Advanced Research Projects Administration, administered by the Army Research Office, (Principal Investigator), "VLSI CAD on Scalable High Performance Computing Platforms," $1,690,000, 1994-98.

- National Science Foundation (Principal Investigator), "Parallel Algorithms for Synthesis and Test," $126,000, 1994-98.
- Office of Naval Research (Principal Investigator) "A Novel Approach to Fault Tolerance in Distributed Memory Multiprocessors," $431,000, 1990-93.
- National Science Foundation (Presidential Young Investigator), "Design Issues in Parallel Processor Architectures," $312,000, 1987-92.
- Semiconductor Research Corporation (Principal Investigator), "Reliable VLSI Architectures," $187,500, 1987-92.
- National Science Foundation, (Principal Investigator), "Fault Tolerant Highly Parallel Signal Processing Architectures," $46,000, 1988-89.
- National Science Foundation, (Principal Investigator), "Parallel Algorithms for VLSI Circuit Extraction on Multiprocessors," $48,000, 1988-89.
- Office of Naval Research (Principal Investigator), "An Algorithmic Approach to Fault Tolerance in Parallel Processors for Space Applications," $60,800, 1988-89.
- General Electric Corporate Research and Development (Principal Investigator), "Parallel Architecture and Algorithms," $37,500, 1987-92.
- National Science Foundation Engineering Research Equipment Grant (Co-principal Investigator with Prof. Wah and Prof. Iyer), "Algorithm Development and Performance Evaluation of Hypercube Multiprocessors, $130,000, 1987-89.
- Intel Scientific Computers (Principal Investigator), "Evaluating Parallel Algorithms on the Intel Hypercube," $50,000, 1987-89.
- IBM Corporation (Principal Investigator), "Parallel Algorithms for VLSI Design Automation," $60,000, 1986-88.

PROFESSIONAL SOCIETIES AND ACTIVITIES:

- Board of Directors, AccelChip, 2000-2003
- Technical Advisory Board, Ambit Design Systems, Santa Clara, CA, 1997-1998.
- Technical Advisory Board, Atrenta, San Jose, CA, 2002-present.
- Technical Advisory Board, Calypto Design Systems, Santa Clara, CA, 2003-present.
- Associate Editor, IEEE Transactions on Parallel and Distributed Systems, 2000-2002.
- Associate Editor, IEEE Transactions on Computers, 1996-2001.
- Associate Editor, Journal of Parallel and Distributed Computing, 1993-2000.
- Associate Editor, IEEE Transactions on VLSI Systems, 1992-1996.
- Associate Editor, Journal of Circuits, Systems and Computers, 1991-1993.
- Editor, Electronic Newsletter on Fault-Tolerant Computing, 1990-92.
- Program Chairman, Int. Conf. High-Performance Computing (HIPC-99), Dec. 1999, Calcutta, INDIA.
- General Chairman, 10th Int. Conf. Parallel and Distributed Computing Systems, New Orleans, Oct. 1997.
- General Chairman, IEEE Int. Workshop on Hardware Fault Tolerance in Multiprocessors, Urbana, 1989.
- Program Chairman, 6th International Conference on High-Performance Computing, Dec. 1999, Calcutta, INDIA.
- Program Chairman, Int. Conf. Parallel Processing (ICPP-95), Oconomowoc, WI, Aug. 1995.
- Program Area Chairman, Int. Symp. Circuits and Systems (ISCAS-93), (Chicago, Illinois, May 1993).
- Advisory Committee, IASTED Conf. Parallel and Distributed Computing Systems (PDCS), Nov. 2002, MIT, Boston, MA
- Advisory Committee, IASTED Conf. Parallel and Distributed Computing Systems (PDCS), Nov. 2001, MIT, Boston, MA
- Program Committee Member, Int. Conference on High Performance Computing, Dec. 2003, Hyderabad, INDIA
- Program Committee Member, International Symp. On Parallel and Dist. Systems (ISPDS), Apr. 2002, Nice, France.
- Program Committee Member, International Conference on Compilers, Architectures and Synthesis of Embedded Systems (CASES), Nov. 2001, Atlanta, GA
- Program Committee Member, Int. Conf. Parallel Processing (ICPP-00), Minneapolis, MN, Aug. 2000.

- Steering Committee Member, 11th International Conference on Parallel and Distributed Computing and Systems (PDCS'99), Boston, MA, Oct. 1999.
- Program Committee Member, Supercomputing Conference (SC-98), Nov. 1998.
- Program Committee Member, 9th Int. Conf. Architectural Support of Programming Languages and Operating Systems, (ASPLOS-98), Santa Clara, CA, Oct. 1998).
- Program Committee Member, Int. Conf. Parallel Processing (ICPP-98), Minneapolis, MN, Aug. 1998.
- Program Committee Member, Int Symp. on Computer Architecture (ISCA-98), Barcelona, Spain, Jun. 1998.
- Program Committee Member, 12th Int. Parallel Processing Symp. (IPPS-98), (Orlando, FL, Apr. 1998)
- Program Committee Member, Workshop on Communication, Architecture, and Applications for Network based Parallel Computing (CANPC 98), (Las Vegas, NE, Feb. 1998).
- Program Committee Member, 10th Int. Conf. on VLSI Design (VLSI-98), (Chennai, INDIA, Jan. 1998).
- Program Committee Member, Int. Conf. Parallel Processing (ICPP-97), (Chicago, IL, Aug. 1997).
- Program Committee Member, 11th Int. Parallel Processing Symp. (IPPS-97), (Geneva, SWITZERLAND, Apr. 1997.)
- Program Committee Member, 9th Int. Conf. on VLSI Design (VLSI-97), (Hyderabad, INDIA, Jan. 1997).
- Program Committee Member, 3rd Int. Conf. High-Performance Computing (ICHPC-96, (Trivandrum, INDIA, Dec. 1996.)
- Program Committee Member, 8th Int. Symp. on Parallel and Distributed Processing (SPDP-96) (New Orleans, LO, Oct. 1996).
- Program Committee Member, 1996 Int. Conf. Parallel Processing (ICPP-96), (Bloomingdale, IL, Aug. 1996).
- Program Committee Member, 3rd Int. Workshop on Parallel Algorithms for Irregularly Structured Problems, (Santa Barbara, CA, Aug. 1996).
- Program Committee Member, 26th Int. Symp. on Fault-Tolerant Computing (FTCS-96), (Sendai, JAPAN, June 1996).
- Program Committee Member, 10th Int. Parallel Processing Symp. (IPPS-96), Honolulu, HA, Apr. 1996. ffl Program and Organizing Committee Member, 8th Int. Conf. on VLSI Design (Bangalore, INDIA, Jan. 1996).
- Program Committee Member, Int. Conf. High Performance Computing, New Delhi, INDIA, Dec. 1995. ffl Program Committee Member, 7th Int. Symp. on Parallel and Distributed Processing (San Antonio, TX, Oct. 1995).
- Program Committee Member, 9th Int. Parallel Processing Symp. (IPPS-95), Santa Barbara, CA, Apr. 1995.
- Program Committee Member, 7th Int. Conf. on VLSI Design (New Delhi, INDIA, Jan. 1995).
- Organizing and Program Committee Member, 21st Int. Symp. on Computer Architecture, (Chicago, IL, May 1994).
- Program Committee Member, 8th Int. Parallel Processing Symp. (IPPS-94), Cancun, Mexico, Apr. 1994.
- Organizing and Program Committee Member, 6th Int. Conf. on VLSI Design (Calcutta, INDIA, Jan. 1994).
- Program Committee Member, 23rd Int. Symp. Fault Tolerant Computing (Tolousse, FRANCE, June 1993).
- Program Committee Member, 5rd Int. Conf. on VLSI Design (Bombay, INDIA, Jan. 1993).
- Program Committee Member, 19th Int. Symp. on Computer Architecture, (Queensland, Australia, May 1992).
- Program Committee Member, Int. Workshop on Fault Tolerance in Parallel and Distributed Systems, (Amherst, MA, Jul. 1992).
- Program Committee Member, 18th Int. Symp. on Computer Architecture (Toronto, CANADA, May 1991).
- Program Committee Member, 5th Int. Parallel Processing Symp. (Orange County, California, Mar. 1991).
- Program Committee Member, 3rd Int. Symp. on VLSI Design (New Delhi, INDIA, Jan. 1991).
- Organizing Committee Member, 19th Int. Symp. Fault-Tolerant Computing (Chicago, June 1989).
- Program Committee Member, 18th Int. Symp. Fault Tolerant Computing (Tokyo, June 1988).
- Presented Tutorial on "Parallel Nonnumerical Algorithms with Applications to VLSI CAD" Int.
- Parallel Processing Symp., Cancun, Mexico, Apr. 1994.
- Presented Tutorial on "Massively Parallel Processing", AT&T (Chicago, June 1993)
- Presented NTU Television Short Course on "Fault Tolerant Multiprocessors", (NTU, May 1994)
- Presented NTU Television Short Course on "Massively Parallel Computing", (NTU, Apr. 1993)
- Presented Tutorial on "Parallel Processing in VLSI Computer-Aided Design Applications," Int. Parallel Processing Symp, (Cancun, Mexico, Apr. 1993).

- Presented Tutorial on "Parallel Processing in VLSI Computer-Aided Design Applications," Int. Conf. Supercomputing, (Washington, DC, Jul. 1992).
- Presented Tutorial on "Introduction to Massively Parallel Processing", Univ. of Illinois Continuing Education, (Chicago, June 1992)
- Presented Tutorial on "Parallel Processing in VLSI Computer-Aided Design Applications," Design Automation Conf. (Orlando, FL, June 1990),
- Presented Tutorial on "Parallel Processing in VLSI Computer-Aided Design Applications," Int. Conf. Computer-Aided Design (Santa Clara, CA, 1988).
- Invited Panelist on “Launching New Products,” ITEC Center, Oct. 2002.
- Invited Panelist on "Program Portability for Parallel Architectures", at IPPS-94 Conference, Cancun, Mexico, Apr. 1994.
- Invited Panelist on "Will Massively Parallel Processing be General Purpose" at IPPS-93 conference, NewPort Beach, Apr. 1993.
- Invited Panelist on "Is Parallel Processing for CAD Real?" at CANDE Workshop, Mar. 1992.
- Panel member, National Science Foundation Panel on Reviewing SBIR Proposals, 1989.
- Session Chairs of various conferences: Int. Parallel Processing Symp (IPPS), 1994, 1993, 1991, Int. Conf. on Computer-Aided Design (ICCAD), 1990, Int. Conf. on Parallel Processing (ICPP), 1994, 1993, 1990, 1988.
- Presented Invited Presentations at Caltech, UCLA, IBM, Texas Instruments, Jet Propulsion Lab, Westinghouse, General Electric, UTexas, Stanford, UIowa, Univ. Minnesota, MIT, Princeton, Univ. Washington, Purdue, Georgia Tech, Northwestern, UC Berkeley.
- Consultant to Westinghouse Corporation, Jet Propulsion Laboratory, Research Triangle Institute, General Electric, United Nations Development Program, AT&T, Integrated Computing Engines, Ambit Design Systems, Atrenta, MediaworksSOC, Calypto Design Systems.

RECENT INVITED LECTURES

- “Compiling Software Binary Programs onto Hardware,” Invited Lecture, Intel Corporation, Santa Clara, CA, Dec.. 2003.
- “An Overview of a Compiler for Compiling MATLAB Programs onto FPGAs,” Invited Lecture, Imperial College, London, ENGLAND, July 2003.
- “An Overview of a Compiler for Compiling MATLAB Programs onto FPGAs,” Invited Lecture, University of Rome, Rome, ITALY, July 2003.
- Invited Speaker on “Overview of the FREEDOM Compiler for Compiling Assembly and Binary Programs onto FPGAs and ASICs.” Cadence Berkeley Labs, Apr. 2003.
- Invited Speaker on “Overview of the FREEDOM Compiler for Compiling Assembly and Binary Programs onto FPGAs and ASICs.” Xilinx, Apr. 2003.
- Invited Speaker on “Technology Commercialization and Entrepreneurship: A Case Study of Accelchip,” Northwestern University, Urbana, May 2003.
- Invited Speaker on “Technology Commercialization and Entrepreneurship: A Case Study of Accelchip,” University of Illinois, Urbana, Apr. 2003.
- Invited Speaker on “Overview of AccelChip” at Chicago Technology Forum, University of Chicago Business School, Oct. 2002.
- Invited Speaker on “Launching Products from a Startup Company: AccelChip,” at Northwestern University, ITEC Center, Oct. 2002.
- “An Overview of the AccelFPGA Compiler for Compiling MATLAB Programs onto FPGAs,” Invited Lecture, University of California, Berkeley, Nov. 2002.
- "An Overview of the AccelFPGA Compiler for Compiling MATLAB Programs onto FPGAs," Indian Institute of Technology, Kharagpur, INDIA, Dec. 2001.
- “Overview of AccelChip” Invited Lecture at University of Illinois, Oct. 2001.
- Electrical and Computer Engineering Distinguished Lecturer, "MATCH: A MATLAB Compilation Environment for Adaptive Computing Systems," University of Toronto, Aug.. 2000.
- Computer and Information Science Distinguished Lecturer, "A MATLAB Compilation Environment for Adaptive Computing Systems," University of California, Irvine, June 2000.

- Electrical and Computer Engineering Outstanding Lecturer, "A MATLAB Compilation Environment for Adaptive Computing Systems," Illinois Institute of Technology, Apr. 2000.
- Electrical and Computer Engineering Distinguished Lecturer, "PROPERCAD: Parallel Algorithms for VLSI CAD" Texas A & M University, Mar. 2000.
- Electrical and Computer Engineering Distinguished Lecturer, "MATCH: A MATLAB Compilation Environment for Adaptive Computing Systems," Texas A & M University, Mar. 2000.
- Computer Science Distinguished Lecturer, "A MATLAB Compilation Environment for Adaptive Com puting Systems," University of Florida, Gainesville, Jan. 1999.
- Keynote Speaker, "Recent Advances in Compilers for Distributed Memory Multicomputers," Int. Conf. on Parallel and Distributed Computing, New Orleans, LO, Oct. 1997.
- Keynote Speaker, "Compiling for Distributed Memory Multicomputers", Int. Workshop on Parallel Processing, Dec. 1994, Bangalore, INDIA.
- Keynote Speaker, "Parallel Algorithms for VLSI CAD", Parallel and Distributed CAD Workshop, part of Fifth Generation Computer Systems Conference, Tokyo, JAPAN, Dec. 1994.
- "A MATLAB Compilation Environment for Adaptive Computing Systems," Invited Lecture, Department of Electrical and Computer Engineering, University of Toronto, July 1998.
- Keynote Speaker, "Recent Advances in Compilers for Distributed Memory Multicomputers," Int. Conf. on Parallel and Distributed Computing, New Orleans, LO, Oct. 1997.
- "The PARADIGM Compiler for Distributed Memory Multicomputers," Invited Lecture, Department of Electrical and Computer Engineering, Indian Institute of Technology, Dec. 1997.
- "ProperCAD: Parallel Algorithms for VLSI CAD" Invited Lecture, Department of Electrical Engineering, University of California, Berkeley, July 1996.
- "The PARADIGM Compiler for Distributed Memory Multicomputers" Invited Lecture, Department of Computer Science, Stanford University, Mar. 1996.
- "The PARADIGM Compiler for Distributed Memory Multicomputers" Invited Lecture, Department of Computer Science, MIT, Oct. 1995.
- "ProperCAD: Parallel Algorithms for VLSI CAD" Invited Lecture, Department of Electrical Engineering, University of Texas at Austin, Aug. 1995.

ADMINISTRATIVE SERVICES TO UNIVERSITY:

- Chairman, Electrical and Computer Engineering Department, Northwestern University, 1998 – 2001 and 2002-present
- Director, Center for Parallel and Distributed Computing, Northwestern University, 1996-present.
- Member, Executive Committee, ECE Department, Northwestern Univer sity, 1996-present.
- Director, Computational Science and Engineering Program, an interdisciplinary program encompassing several engineering and science departments in the University of Illinois, 1994-1996.
- Chairman, Computer Engineering Area Committee, ECE Dept, 1991-94.
- Chairman, Illinois Computer Affiliates Program, 1991-92.
- Member, ECE Department Faculty Search Committee, 1995-96.
- Member, College Steering Committee on Computational Science and Engineering Program, 1993-94.
- Member, Curriculum Committee, ECE Department, 1988-90.
- Member, ABET Committee, ECE Department, 1988-90.

MAJOR AREAS OF RESEARCH:

1. Compilers for Adaptive Computing
2. Compilers for Low Power Computing
3. Compiling Software Binaries to Hardware.
4. Parallel Algorithms for VLSI Computer-Aided Design Applications
5. Parallelizing Compilers for Distributed Memory Multiprocessors

TEACHING EXPERIENCE:

- Started and taught the following courses at Northwestern University: Introduction to Parallel Computing (ECE C58) Advanced Digital Design (ECE C03) Parallel Algorithms for VLSI Computer-Aided Design (ECE D58)
- Taught the following courses at the University of Illinois: Introduction to VLSI Systems Design (ECE325) VLSI Design Projects (ECE326) Microcomputer Design Laboratory (ECE311) Design of Fault-Tolerant Digital Systems (ECE442) Introduction to Computer Engineering (ECE290). Parallel Algorithms for VLSI CAD (ECE 426). Introduction to Parallel Programming (ECE 392).
- Introduction to Parallel Programming, a 5-day short course at the Computational Material Science Summer School, University of Illinois, Aug. 1996.
- Introduction to Massively Parallel Processing, a 2-day short course at AT&T, July 1992, and June 1993.
- Massively Parallel Computing, a 2-day Satellite TV short course offered through National Technological University (NTU), April 1993.
- Fault Tolerant Multiprocessors, a 4 day short course at AT&T, Aug. 1993. Use of Parallel Processing for VLSI CAD, one-day tutorial at the IEEE Int. Conf. on Supercomputing, Washington, DC, 1992.
- Introduction to Massively Parallel Processing, a 2-day short course at the Du Page County professionals through the Continuing Education program of University of Illinois, Jun. 1992.
- Programming Parallel Processors, 2-week course arranged by United Nations Development Program at the Indian Institute of Science, Bangalore, INDIA, 1991, attended by 50 professionals in India.
- Fault Tolerant Computing, 16 week course at AT&T, Naperville, IL, Fall 1990, attended by 50 AT&T employees.
- Parallel Processing for VLSI CAD, one-day tutorial at the IEEE Int. Conf. on Computer-Aided Design, Santa Clara, CA, 1988, 100 professional attendees.
- Parallel Algorithms for VLSI CAD, one-day tutorial ACM/IEEE Design Automation Conference, Orlando, FL, 1990, 120 professional attendees.
- Parallel Algorithms for VLSI CAD, one-day tutorial Int. Parallel Processing Symp., Cancun, Mexico, Apr. 1994.

GRADUATE STUDENT SUPERVISION:

Postdoctoral Student Supervised: 1

1. B. Ramkumar, PROPERCAD: A Portable Object Oriented Parallel Environment for VLSI CAD, Jan. 1991-Aug. 1992.

Ph.D. Theses Supervised: 33

1. A. L. N. Reddy, "Parallel Input/Output Architectures for Multiprocessors," CRHC-90-5, UILU-ENG-90-2235, UIUC Ph.D. Thesis, ECE Department, May 1990.

2. R. M. Kling "Optimization by Simulated Evolution and Its Application to Cell Placement," CRHC-90-7, UILU-ENG-90-2237, UIUC Ph.D. Thesis., ECE Department, May 1990.

3. S. Patil "Parallel Algorithms for Test Generation and Fault Simulation," CRHC-90-12, UILU-ENG-90-2245, UIUC Ph.D. Thesis, ECE Department, August 1990.

4. K. P. Belkhale "Parallel Algorithms for Computer-Aided Design with Applications to Circuit Extraction," CRHC-90-15, UILU-ENG-90-2252, UIUC Ph.D. Thesis, CS Department, August 1990.

5. V. Balasubramanian, "Analysis and Synthesis of Algorithm Based Error Detection in Multiprocessors," CRHC-91-6, UIUC PhD Thesis, ECE Department, Feb. 1991.

6. R. Brouwer, "Parallel Algorithms for Placement and Routing," CRHC-91-2, UIUC PhD Thesis, ECE Department, Feb. 1991.

7. J. M. Hsu, “Performance Evaluation and Hardware Support of Message Communication in Distributed Memory Multicomputers,” CRHC-91-5, UIUC PhD Thesis, CS Department, Feb. 1991.

8. M. Gupta, “Automated Data Partitioning in Distributed Memory Multicomputers,” UIUC PhD Thesis, CS Department, September 1992.

9. S. Kim, “Novel Algorithms for Cell Placement and Their Parallel Implementations,” UIUC PhD Thesis, ECE Department, July 1993.

10. K. De, “Parallel Algorithms for Logic Synthesis,” UIUC PhD Thesis, ECE Department, September 1993.

11. S. Parkes, “A Class Library Approach to Concurrent Object-Oriented Programming with Applications to VLSI CAD,” UIUC Ph.D. Thesis, ECE Department, September 1994.

12. M. Peercy, “Design of Hardware and Software Reconfiguration Strategies for Distributed Memory Multicomputers, “, UIUC Ph.D Thesis, ECE Department, September 1994.

13. A. Lain, “Compiler and Runtime System for Supporting Irregular Applications in Distributed Memory Multicomputers,” UIUC Ph.D. Thesis, CS Department, October 1995.

14. A. Roy-Chowdhury, “Manual and Compiler Assisted Techniques for Synthesizing Fault-Tolerant Parallel Programs,” UIUC Ph.D. Thesis, ECE Department, November 1995.

15. S. Ramaswamy, “Simultaneous Exploitation of Task and Data Parallelism in Regular Scientific Applications,” UIUC Ph.D. Thesis, ECE Department, January 1996.

16. D. Palermo, “Compiler Techniques for Optimizing Communication and Data Distribution in Distributed Memory Multicomputers,” UIUC Ph.D. Thesis, ECE department, May 1996.

17. J. Chandy, “Parallel Algorithms for Standard Cell Placement Using Simulated Annealing,” UIUC Ph.D. Thesis, ECE department, July 1996.

18. E. Su, “A Compilation Framework for Distributed Memory Message-Passing Multicomputers,” UIUC Ph.D. Thesis, ECE department, Mar. 1997.

19. J. Holm, “Performance Evaluation of Message-Driven Parallel Applications on General-Purpose Multiprocessors,” UIUC Ph.D. Thesis, ECE department, Apr. 1997.

20. V. Krishnaswamy, “Parallel Algorithms for VHDL Simulation,” UIUC Ph.D. Thesis, CS department, Apr. 1997.

21. Z. Xing, Novel Algorithms for Placement and Routing and their Parallel Implementations, UIUC Ph.D. Thesis, CS department, Jul. 1997.

22. D. Krishnaswamy, “Parallel Algorithms for Test Generation and Fault Simulation,” UIUC Ph.D. Thesis, ECE department, Jul. 1997.

23. G. Hasteer, “Equivalance Checking in a Modular Checking Framework,” UIUC Ph.D. Thesis, CS department, Dec. 1997.

24. S. Roy, “Low Power Driven Sequential Algorithms for Combinational and Sequential Circuits,” UIUC Ph.D. Thesis, ECE Department, Aug. 1998.

25. P. Prabhakaran, “Improved Algorithms for High-Level Synthesis and Their Parallel Implementations,” UIUC Ph.D. Thesis, CS department, Oct. 1998.

26. D. Chakrabarti, "Design and Evaluation of a Uniform Compilation Framework for Hybrid Applications, " Northwestern Univ. ECE Department, June 2000.

27. Y. Yuan, "Novel Algorithms for 3-D Capacitance Extraction and the Parallel Implementations," Northwestern Univ. ECE Department, June 2000.

28. M. Haldar, "Optimized Hardware Synthesis for FPGAs," Northwestern University, ECE Department, Aug. 2001.

29. A. Nayak, "Automatic Parallelization and Optimizations for Synthesizing MATLAB Programs on Multi FPGA Systems," Northwestern University, ECE Department, Aug. 2001.

30. A. K. Jones, "PACT HDL: A C Compiler with Power and Performance Optimizations,"Northwestern University, ECE Department, Aug. 2002.

31. Pramod Joisha, "A Type Inferencing System for MATLAB," Northwestern University, ECE Department, Aug. 2003.

32. Xiaoyong Tang, "High-Level Synthesis Algorithms for Low Power ASIC Design," Northwestern University, ECE Department, June 2004.

33. Tianyi Jiang, "Power Aware High-level Sythnesis Techniques for FPGAs," Northwestern University, ECE Department, June 2004.

M.S. Theses Supervised: 39

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Currently Supervising 8 Ph.D. candidates at Northwestern.

- Gaurav Mittal, Algorithms for Binary Translation, Ph.D. expected 2004.
- David Zaretsky, Compilation of DSP Algorithms to FPGAs, Ph.D. expected 2004.
- Nikos Liveris, System-Level Verification Algorithms, Ph.D. expected 2005.
- Rajarshi Mukherjee, System-Level Verification Algorithms, Ph.D. expected 2005.
- Sanghamitra Roy, Automated Conversion of Floating Point Computations to Fixed Point Computations in MATLAB, Ph.D. expected 2006.

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- K. P. Belkhale, went to IBM, now at Cadence Design Systems
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- M. Gupta, IBM
- S. Kim, went to LSI Logic, now at Synopsys
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- S. Parkes, started own company, Sierra Vista Research, now at IBM Almaden
- M. Peercy, IBM

- A. Lain, Hewlett-Packard
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- S. Ramaswamy, IBM
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- G. Hasteer, Cadence Design Systems
- S. Roy, Cadence Design Systems
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UNIVERSITIES WHERE FORMER Ph.D. STUDENTS ARE WORKING:

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- J. Chandy, University of Connecticut
- A. K. Jones, University of Pittsburg

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PATENT APPLICATIONS

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SUMMARY OF INFORMATION

Prith Banerjee received his B.Tech. degree in Electronics and Electrical Engineering from the Indian Institute of Technology, Kharagpur, India, in August 1981, and the M.S. and Ph.D degrees in Electrical Engineering from the University of Illinois at Urbana-Champaign in December 1982 and December 1984 respectively.

Dr. Banerjee is currently the Walter P. Murphy Professor and Chairman of the Department of Electrical and Computer Engineering, and Director of the Center for Parallel and Distributed Computing. at Northwestern University in Evanston, Illinois. Prior to that he was the Director of the Computational Science and Engineering program, and Professor of Electrical and Computer Engineering and the Coordinated Science Laboratory at the University of Illinois at Urbana-Champaign.

Prith Banerjee has also served as Founder, President and CEO of a company called AccelChip during 2000- 2002 while he was on leave from Northwestern University. This company was founded based on technology developed as part of a DARPA sponsored research on the MATCH compiler at Northwestern. Subsequently, he served AccelChip as Chief Scientist during 2002-2004.

Dr. Banerjee's research interests are in Parallel Algorithms for VLSI Design Automation, Distributed Memory Parallel Compilers, and Compilers for Adaptive Computing, and is the author of over 300 papers in these areas. He leads the PARADIGM compiler project for compiling programs for distributed memory multicomputers, the ProperCAD project for portable parallel VLSI CAD applications, the MATCH project on a MATLAB compilation environment for adaptive computing, and the PACT project on power aware compilation of hardware and software . He is also the author of a book entitled "Parallel Algorithms for VLSI CAD" published by Prentice Hall, Inc., 1994.

Dr. Banerjee has received numerous awards and honors during his career. He became a Fellow of the ACM in 2000. He was the recipient of the 1996 Frederick Emmons Terman Award of ASEE's Electrical Engineering Division sponsored by Hewlett-Packard. He was elected to the Fellow grade of IEEE in 1995. He received the University Scholar award from the University of Illinois for in 1993, the Senior Xerox Research Award in 1992, the IEEE Senior Membership in 1990, the National Science Foundation's Presidential Young Investigators' Award in 1987, the IBM Young Faculty Development Award in 1986, and the President of India Gold Medal from the Indian Institute of Technology, Kharagpur, in 1981.

Dr. Banerjee has served as the Program Chair of the High-Performance Computing Conference in 1999, and Program Chair of the Int. Conf. on Parallel Processing for 1995. He has served as General Chairman of the International Conference on Parallel and Distributed Computing Systems in 1997, and the International Workshop on Hardware Fault Tolerance in Multiprocessors, 1989. He has served on the Program and Organizing Committees of the 1988, 1989, 1993 and 1996 Fault Tolerant Computing Symposia, the 1992, 1994, 1995, 1996 and 1997 International Parallel Processing Symposium, the 1991, 1992, 1994 and 1998 International Symposia on Computer Architecture, the 1998 International Conference on Architectural Support of Programming Languages and Operating Systems, the 1990, 1993, 1994, 1995, 1996, 1997 and 1998 International Symposium on VLSI Design, the 1994, 1995, 1996, 1997, 1998 and 2000 International Conference on Parallel Processing, and the 1995, 1996 and 1997 International Conference on High-Performance Computing. He is an Associate Editor of the IEEE Transactions on Parallel and Distributed Systems, and IEEE Transactions on Computers. In the past he has served as Associate Editor of the Journal of Parallel and Distributed Computing, the IEEE Transactions on VLSI Systems, and the Journal of Circuits, Systems and Computers.

Prith has served on the Technical Advisory Board of many companies such as Ambit Design Systems, Calypto Design Systems, and Atrenta.

Prith has received research grants worth about $4.0 million during his 12 years at Illinois with him as a principal investigator. He has received about $8.0 million at Northwestern University during the past 4 years. His funding has come from national agencies such as DARPA, NSF, ONR, NASA and industries such as IBM, Intel, General Electric, and SRC.

He has completed the supervision of 33 Ph.D. and 39 M.S. students already, and is presently supervising 4 Ph.D. students.

SUMMARY OF RESEARCH

Professor Prith Banerjee has performed research on Parallel Algorithms, Parallel Compilers, and Parallel Architectures, and Compilers for Adaptive Computing. He has published over 300 papers in premier journals and conferences. In the following, his main research accomplishments are summarized.

(1) Parallel Algorithms for VLSI CAD. As VLSI circuits become more complex, the computational requirements for performing various CAD tasks increase almost exponentially. Professor Banerjee has investigated efficient parallel algorithms for various tasks in VLSI computer-aided design in order to reduce the runtimes of these tools for future billion transistor VLSI chips from weeks to hours. He has written a graduate level textbook on the subject, "Parallel Algorithms for VLSI CAD," published by Prentice Hall, 1994. As part of the PROPERCAD project, he has developed portable parallel algorithms that are suitable for execution on distributed memory message-passing multicomputers, networks of workstations, and shared-memory multiprocessors. His most significant publications in this area include his work on parallel simulated annealing algorithms for standard cell placement where he proposed and evaluated several parallel strategies such as parallel moves, speculative computation and multiple markov chains approaches. In his work on parallel algorithms for test generation of combinational and sequential circuits, he proposed how a parallel branch and bound algorithm for test generation can be efficiently integrated within a parallel fault simulation environment. He has worked on parallel circuit extraction and design rule checking, where he developed strategies for exploiting data parallelism on flattened layouts, and task parallelism on hierarchical layouts, and sophisticated scheduling for combining task and data parallelism. He has also worked on parallel algorithms for global and detailed routing using iterative improvement, parallel algorithms for combinational and sequential logic synthesis using the MIS and transduction algorithms, parallel algorithms for behavioral simulation using VHDL, and on parallel algorithms for high-level synthesis. Dr. Banerjee published more than 100 papers in this area; two of these papers have received the Best Paper Awards at conferences, one for his work on "SPITFIRE: Scalable Parallel Algorithms for Test Set Partitioned Fault Simulation" at the IEEE VLSI Test Symposium in 1997, and another for his work on "A Parallel Implementation of A Fast Multipole Based 3-D Capacitance Extraction Program on Distributed Memory Multicomputers" at the IEEE Int. Parallel and Distributed Symposium in 2000. Prith's work in this area was supported by DARPA, NSF, and the Semiconductor Research Corporation. He has worked closely with many companies including the Cadence, LSI Logic, Ambit Design Systems, and Sunrise Test Systems, to develop these parallel algorithms and have transferred many of these algorithms to industry. For example, LSI Logic has a commercial product called Parallel Gate-Ensemble which is based on the parallel cell placement algorithms developed by him. Cadence Design Systems has a product called parallel VAMPIRE which is based on some of the parallel design rule checking algorithms developed by him. Finally, he has worked with Ambit Design Systems to develop a product called Distributed Buildgates for parallel logic synthesis. The Design Sciences Program of the Semiconductor Research Corporation listed the ProperCAD project under Professor Banerjee as one of the two key Technical Innovations during the 1994 year, and was included in the SRC Corporate Annual Report. More information about the ProperCAD project can be found at: http:/www.ece.nwu.edu/cpdc/ProperCAD/pcad.html.

(2) Parallelizing Compilers. Distributed memory message passing machines such as the Intel Paragon, and the IBM SP-2 and networks of workstations offer significant advantages over shared-memory multiprocessors in terms of cost and scalability. Unfortunately, to extract all that computational power from these machines, users have to write efficient software for them, which is an extremely laborious process. As part of the PARADIGM compiler project, Prof. Banerjee has developed strategies by which sequential programs written in Fortran 77 or High Performance Fortran can be automatically parallelized and compiled for efficient execution on distributed memory message-passing multicomputers and networks of workstations. His most significant publications in this area include his work on automated data distribution on distributed memory multi-processors, where he developed a constraint-based approach for deriving the static and dynamic distributions of regular data structures using simple computation and communication cost models. He has also developed strategies where the PARADIGM compiler can automatically extract data and functional parallelism simultaneously from Fortran programs using a convex programming formulation. His other significant contribution is in the development of an uniform framework for supporting both regular and irregular data accesses using an interval based runtime library using the inspector-executor approach. He has recently developed strategies for unified loop and data transformations for improving cache locality in distributed shared memory multiprocessors. Prith's work on the PARADIGM compiler is one of five leading research projects in academia in this area of parallelizing compilers fordistributed memory multiprocessors; this includes Ken Kennedy's work on the Fortran D compiler at Rice, Monica Lam's work on SUIF at Stanford, Joel Saltz's work on CHAOS/PARTI

at Maryland, David Padua's work on the Polaris compiler at Illinois, and Hans Zima's work on the Vienna Fortran compiler in Europe. Prith's work has been supported by DARPA, NSF and various companies. He has published more than 80 papers in this area (out of 270 total papers in his career), one of which received a Best Paper Award at the International Conference on Parallel Processing in 1994 for the paper entitled "Communication Optimizations for Distributed Memory Multicomputers in the PARADIGM Compiler." He has worked closely with many companies including IBM, Kuck and Associates, and Portland Group, to develop various compiler techniques, and has transferred many of these techniques to industry. Specifically, the automatic data partitioning and static cost estimation work was transferred to IBM T.J. Watson Center (by Manish Gupta) in the IBM xlf HPF compiler. The PARADIGM compiler has been licensed to a company, Tata Information Systems Ltd., for commercial development. More information about the PARADIGM project can be found at: http:/www.ece.nwu.edu/cpdc/Paradigm/Paradigm.html

(3) MATLAB Compiler for Reconfigurable Computing. Digital signal processing and image processing applications are typically written in the MATLAB programming language, and are typically executed on general purpose DSP processors. However, recently DSP algorithms are being mapped onto Reconfigurable Field Programmable Gata Arrays (FPGAs) for performance and reconfigurability reasons. However, to map DSP algorithms onto FPGAs, users are required to manually translate MATLAB programs onto languages such as VHDL or Verilog. As part of the MATCH project, Professor Banerjee has the MATCH compiler that takes MATLAB programs and automatically parallelizes it and maps it a heterogeneous environment of off-the-shelf embedded processors, digital signal processors, and FPGAs. More details of the MATCH project can be found at the URL: http://www.ece.nwu.edu/cpdc/Match/Match.html. He has transferred this technology to a new company he has founded called Accelchip (www.accelchip.com) which has developed a successful product called AccelFPGA based on the MATCH compiler.

(4) Compiler for Power Aware Computing. Low power electronic circuits are becoming very desirable in the domain of mobile wireless devices. Current electronic design tools have two limitations: (1) They require the designers to enter their designs at the register transfer level in languages such as VHDL or Verilog (2) They perform area minimizations under timing constraints or perform timing optimizations under area constraints. As part of the PACT compiler project, Prith Banerjee is developing a compiler that will take a high-level language, namely, C, and automatically produce Register Transfer Level VHDL and Verilog code that can be mapped onto FPGAs and ASICs. Furthermore, this transformation will be performed under power, area and timing constraints. More details of the MATCH project can be found at the URL: http://www.ece.nwu.edu/cpdc/PACT/PACT.html

(5) Compiling Software Binaries onto Hardware. Increasing demands for cell-phones, PDAs, and network devices have provided opportunities for the growth of embedded software, operating systems and development tools. As newer processor architectures are announced, there is a need to reuse and migrate the software from older generation processors to newer processors. In this research we will develop automated compiler algorithms to translate software binary and assembly code of a general-purpose processor into Register Transfer Level VHDL and Verilog code to be mapped onto hardware in the form of FPGAs and ASICsWe further plan to study techniques for performing hardware/software co-design and verification on integrated Systems-on-a-Chip (SOC) platforms consisting of embedded processors, memories, FPGAs and ASICs. We are demonstrating our concepts using a prototype FREEDOM compiler that will translate binary code of a Texas Instruments TMS320 C6000 processor into a hardware/software implementation on a Xilinx Virtex II Pro SOC. More details of the FREEDOM project can be found at the URL: http://www.ece.nwu.edu/cpdc/FREEDOM/FREEDOM.html

CONTRIBUTIONS AS AN ADMINISTRATOR

Prith Banerjee has had wide ranging experience as an administrator. He has served as

- Director the Computational Science and Engineering Program at the University of Illinois from 1994 to 1996.
- Director of the Center for Parallel and Distributed Computing at Northwestern University from 1996-present
- Chairman of the Electrical and Computer Engineering department at Northwestern University from 1998-2001 and 2002-present

- President and CEO of AccelChip from 2000 to 2002.

In the following his contributions as an administrator will be described in more detail.

Prith Banerjee was instrumental in the development of a new graduate program at the University of Illinois called Computational Science and Engineering. The term Computational Science and Engineering (CSE) refers to those activities in science and engineering that exploit computing as their main tool. The purpose of the graduate option in CSE at the University of Illinois was to develop an academic program that prepares students with an interdisciplinary background in numerical computing, high performance software and parallel computing, and computational aspects of various applications. Prof. Banerjee was the founding Director of the CSE program at Illinois during 1994-96. During those two years, he was successful in establishing the CSE academic program in ten departments, creating/identifying more than 40 CSE courses, sponsoring 8 research assistantships for CSE research activities, writing research proposals to obtain advanced computing equipment for a CSE laboratory, starting a CSE seminar, and writing proposals to acquire grants for research in CSE. Through his efforts, he was able to procure the donation of 10 workstations from IBM, and a 24 processor Paragon multiprocessor from Intel, a SUN Sparcserver 8 processor multiprocessor, and a dozen SUN workstations.

Since Sep. 1, 1996, Prof. Banerjee has been the Director of the Center for Parallel and Distributed Computing at Northwestern University. The Center has 11 faculty from Northwestern and two scientists from Argonne National Lab. The Center has attracted three large DARPA grants worth about $2 million each, namely the MATCH compiler project, the CHIMAERA project, and the PACT compiler project. In addition, he has brought in a $1 million NSF grant on the PANTHER project, and a $1 million DOE grant to support research on a wide range of topics in high-performance computing.

During Sep. 1, 1998 to Aug. 31, 2001, and from September 1, 2002 to present, Prof. Banerjee has been the Chairman of the Electrical and Computer Engineering Department at Northwestern University. During these five years, he has led the development of some innovative revisions of the electrical engineering and computer engineering undergraduate curricula at Northwestern. He has been responsible for leading the creation of two freshman courses ECE 202 on "Introduction to Electrical Engineering" and ECE 203 on "Introduction to Computer Engineering". The ECE 202 course teaches electrical engineering to freshman students using the design of a CD player, and the ECE 203 course teaches computer engineering to freshmen using the design of an autonomous robot. During 1998-99, he personally attended weekly meetings of two committees, the undergraduate electrical engineering committee, and the undergraduate computer engineering committee, which designed the new curriculum and the courses. He has also been instrumental in making major renovations in the instructional labs of the department by securing equipment donations from companies such as Hewlett-Packard, Motorola and Microsoft, and obtaining significant funding from the President of Northwestern University. In addition, he was instrumental in hiring 11 new faculty in the department (including 2 women), 6 of whom have won the NSF CAREER awards. During this period the rankings of the ECE Department have gone up to 17th in Computer Engineering and 20th in Electrical Engineering according to US News and World Reports.

CONTRIBUTIONS AS AN ENTREPRENEUR

Dr. Banerjee has founded a company called AccelChip, located in Schaumburg, Illinois (www.accelchip.com) in July 2000. He served as its Founder, President and CEO until June 2002. During July, 2002 to June 2004, he transitioned to the role of Chief Scientist in a part time consulting role. The company has developed its first product called AccelFPGA which takes MATLAB and SIMULINK versions of DSP applications and map into field programmable gate arrays (FPGAs) This technology is based on the MATCH compiler technology developed at Northwestern University. Over the past two years he has hired a top management team, has raised $2.3 million in Venture Capital funding, and produced over $800,000 in revenues of its products, and grown the company to more than 20 employees. He was on leave from Northwestern University during 2001-2002, and has gone back to Northwestern as Chairman of the ECE department effective September 1, 2002.