# The "Millipede"—More than one thousand tips for future AFM data storage

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**We report on a new atomic force microscope (AFM)-based data storage concept called the "Millipede" that has a potentially ultrahigh density, terabit capacity, small form factor, and high data rate. Its potential for ultrahigh storage density has been demonstrated by a new thermomechanical local-probe technique to store and read back data in very thin polymer films. With this new technique, 30–40-nm-sized bit indentations of similar pitch size have been made by a single cantilever/tip in a thin (50-nm) polymethylmethacrylate (PMMA) layer, resulting in a data storage density of 400–500 Gb/in.$^2$ High data rates are achieved by parallel operation of large two-dimensional (2D) AFM arrays that have been batch-fabricated by silicon surface-micromachining techniques. The very large scale integration (VLSI) of micro/nanomechanical devices (cantilevers/tips) on a single chip leads to the largest and densest 2D array of 32 × 32 (1024) AFM cantilevers with integrated write/read storage functionality ever built. Time-multiplexed electronics control the write/read storage cycles for parallel operation of the Millipede array chip. Initial areal densities of 100–200 Gb/in.$^2$ have been achieved with the 32 × 32 array chip, which has potential for further improvements. In addition to data storage in polymers or other media, and not excluding magnetics, we envision areas in nanoscale science and technology such as lithography, high-speed/large-scale imaging, molecular and atomic manipulation, and many others in which Millipede may open up new perspectives and opportunities.**

## 1. Introduction, motivation, and objectives

In the 21st century, the nanometer will very likely play a role similar to the one played by the micrometer in the 20th century. The nanometer scale will presumably pervade the field of data storage. In magnetic storage today, there is no clear-cut way to achieve the nanometer scale in all three dimensions. The basis for storage in the 21st century might still be magnetism. Within a few years, however, magnetic storage technology will arrive at a stage of its exciting and successful evolution at which fundamental changes are likely to occur when current storage technology hits the well-known superparamagnetic limit. Several ideas have been proposed on how to overcome





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this limit. One such proposal involves the use of patterned magnetic media, for which the ideal write/read concept must still be demonstrated, but the biggest challenge remains the patterning of the magnetic disk in a cost-effective way. Other proposals call for totally different media and techniques such as local probes or holographic methods. In general, if an existing technology reaches its limits in the course of its evolution and new alternatives are emerging in parallel, two things usually happen: First, the existing and well-established technology will be explored further and everything possible done to push its limits to take maximum advantage of the considerable investments made. Then, when the possibilities for improvements have been exhausted, the technology may still survive for certain niche applications, but the emerging technology will take over, opening up new perspectives and new directions.

Consider, for example, the vacuum electronic tube, which was replaced by the transistor. The tube still exists for a very few applications, whereas the transistor evolved into today's microelectronics with very large scale integration (VLSI) of microprocessors and memories. Optical lithography may become another example: Although still the predominant technology, it will soon reach its fundamental limits and be replaced by a technology yet unknown. Today we are witnessing in many fields the transition from structures of the micrometer scale to those of the nanometer scale, a dimension at which nature has long been building the finest devices with a high degree of local functionality. Many of the techniques we use today are not suitable for the coming nanometer age; some will require minor or major modifications, and others will be partially or entirely replaced. It is certainly difficult to predict which techniques will fall into which category. For key areas in information technology hardware, it is not yet obvious which technology and materials will be used for nanoelectronics and data storage.

In any case, an emerging technology being considered as a serious candidate to replace an existing but limited technology must offer long-term perspectives. For instance, the silicon microelectronics and storage industries are huge and require correspondingly enormous investments, which makes them long-term-oriented by nature. The consequence for storage is that any new technique with better areal storage density than today's magnetic recording [1] should have long-term potential for further scaling, desirably down to the nanometer or even atomic scale.

The only available tool known today that is simple and yet provides these very long-term perspectives is a nanometer sharp tip. Such tips are now used in every atomic force microscope (AFM) and scanning tunneling microscope (STM) for imaging and structuring down to the atomic scale. The simple tip is a very reliable tool that concentrates on one functionality: the ultimate local confinement of interaction.

In the early 1990s, Mamin and Rugar at the IBM Almaden Research Center pioneered the possibility of using an AFM tip for readback and writing of topographic features for the purposes of data storage. In one scheme developed by them [2], reading and writing were demonstrated with a single AFM tip in contact with a rotating polycarbonate substrate. The data were written thermomechanically via heating of the tip. In this way, densities of up to 30 Gb/in.$^2$ were achieved, representing a significant advance compared to the densities of that day. Later refinements included increasing readback speeds to a data rate of 10 Mb/s [3] and implementation of track servoing [4].

In making use of single tips in AFM or STM operation for storage, one must deal with their fundamental limits for high data rates. At present, the mechanical resonant frequencies of the AFM cantilevers limit the data rates of a single cantilever to a few Mb/s for AFM data storage [5, 6], and the feedback speed and low tunneling currents limit STM-based storage approaches to even lower data rates.

Currently a single AFM operates at best on the microsecond time scale. Conventional magnetic storage, however, operates at best on the nanosecond time scale, making it clear that AFM data rates have to be improved by at least three orders of magnitude to be competitive with current and future magnetic recording.

The objectives of our research activities within the Micro- and Nanomechanics Project at the IBM Zurich Research Laboratory are to explore highly parallel AFM data storage with areal storage densities far beyond the expected superparamagnetic limit (60–100 Gb/in.$^2$) [7] and data rates comparable to those of today's magnetic recording.

The "Millipede" concept presented here is a new approach for storing data at high speed and with an ultrahigh density. It is not a modification of an existing storage technology, although the use of magnetic materials as storage media is not excluded. The ultimate locality is given by a tip, and high data rates are a result of massive parallel operation of such tips. Our current effort is focused on demonstrating the Millipede concept with areal densities up to 500 Gb/in.$^2$ and parallel operation of very large 2D ($32 \times 32$) AFM cantilever arrays with integrated tips and write/read storage functionality.

The fabrication and integration of such a large number of mechanical devices (cantilever beams) will lead to what we envision as the VLSI age of micro- and nanomechanics. It is our conviction that VLSI micro/nanomechanics will greatly complement future micro- and nanoelectronics (integrated or hybrid) and

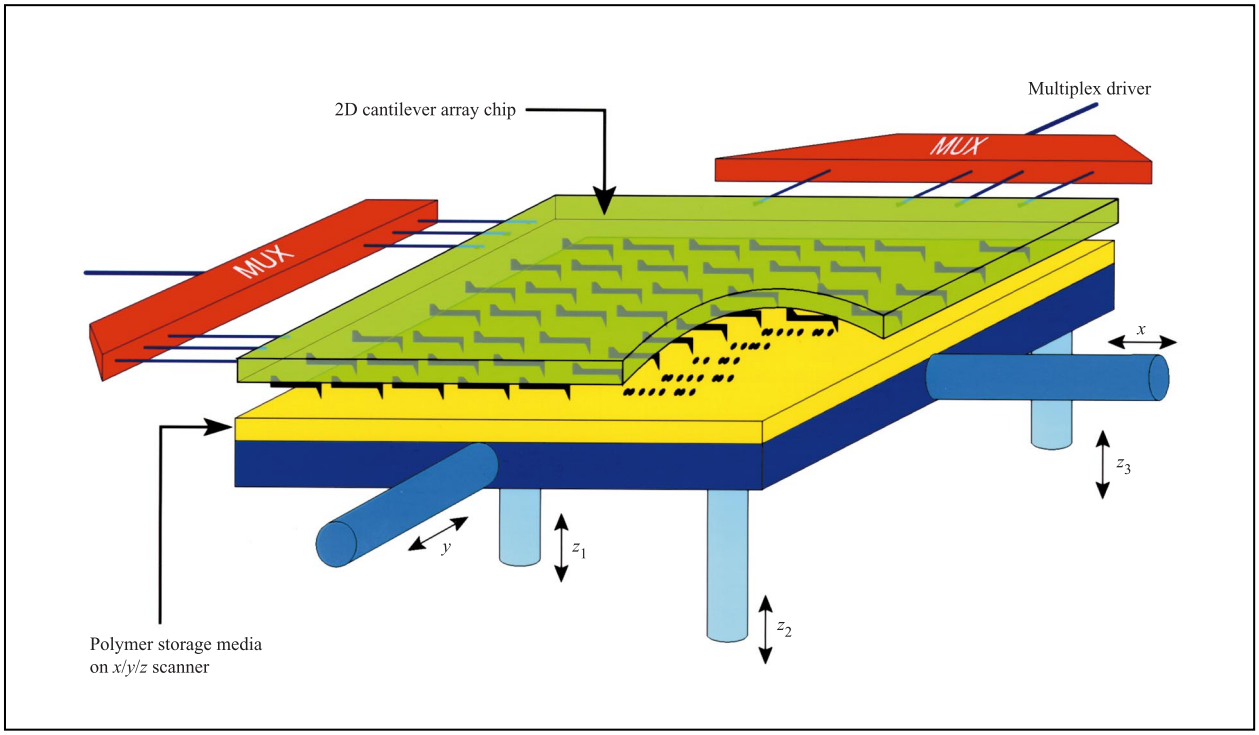



Figure 1

"Millipede" concept. From [17(a)], reproduced with permission; © 1999 IEEE.

may generate applications of VLSI–Nano(Micro) ElectroMechanical Systems [VLSI–N(M)EMS] not conceived of today.

## 2. The Millipede concept

The 2D AFM cantilever array storage technique [8, 9] called "Millipede" is illustrated in **Figure 1**. It is based on a mechanical parallel *x*/*y* scanning of either the entire cantilever array chip or the storage medium. In addition, a feedback-controlled *z*-approaching and -leveling scheme brings the entire cantilever array chip into contact with the storage medium. This tip–medium contact is maintained and controlled while *x*/*y* scanning is performed for write/read. It is important to note that the Millipede approach is not based on individual *z*-feedback for each cantilever; rather, it uses a feedback control for the entire chip, which greatly simplifies the system. However, this requires stringent control and uniformity of tip height and cantilever bending. Chip approach and leveling make use of four integrated approaching cantilever sensors in the corners of the array chip to control the approach of the chip to the storage medium. Signals from three sensors (the fourth being a spare) provide feedback signals to adjust three magnetic *z*-actuators until the three approaching sensors are in contact with the medium. The three sensors with the individual feedback loop maintain the chip leveled and in contact with the surface while *x*/*y* scanning is performed for write/read operations. The system is thus leveled in a manner similar to an antivibration air table. This basic concept of the entire chip approach/leveling has been tested and demonstrated for the first time by parallel imaging with a 5 × 5 array chip [10]. These parallel imaging results have shown that all 25 cantilever tips have approached the substrate within less than 1 $\mu$m of *z*-activation. This promising result has led us to believe that chips with a tip-apex height control of less than 500 nm are feasible. This stringent requirement for tip-apex uniformity over the entire chip is a consequence of the uniform force needed to minimize or eliminate tip and medium wear due to large force variations resulting from large tip-height nonuniformities [4].

During the storage operation, the chip is raster-scanned over an area called the storage field by a magnetic *x*/*y* scanner. The scanning distance is equivalent to the cantilever *x*/*y* pitch, which is currently 92 $\mu$m. Each cantilever/tip of the array writes and reads data only in its own storage field. This eliminates the need for lateral

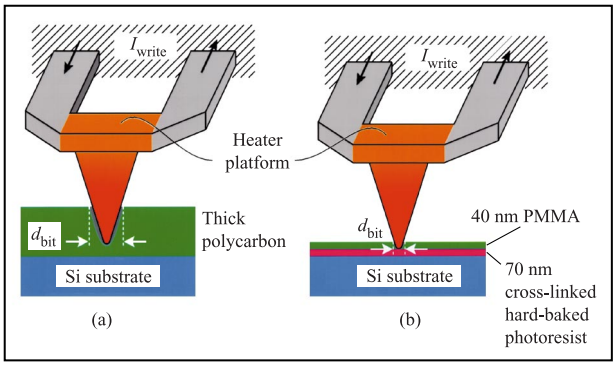



Figure 2

(a) Earlier storage medium consisting of a bulk polycarbonate layer. (b) New storage medium for smaller bit sizes, consisting of a thin writable PMMA layer on top of a Si substrate separated by a cross-linked film of photoresist. From [12], reproduced with permission.

positioning adjustments of the tip to offset lateral position tolerances in tip fabrication. Consequently, a 32 × 32 array chip will generate 32 × 32 (1024) storage fields on an area of less than 3 mm × 3 mm. Assuming an areal density of 500 Gb/in.$^2$, one storage field of 92 $\mu$m × 92 $\mu$m has a capacity of about 10 Mb, and the entire 32 × 32 array with 1024 storage fields has a capacity of about 10 Gb on 3 mm × 3 mm. As shown in Section 7, the storage capacity scales with the number of elements in the array, cantilever pitch (storage-field size) and areal density, and depends on the application requirements. Although not yet investigated in detail, lateral tracking will also be performed for the entire chip, with integrated tracking sensors at the chip periphery. This assumes and requires very good temperature control of the array chip and the medium substrate between write and read cycles. For this reason the array chip and medium substrate should be held within about 1°C operating temperature for bit sizes of 30 to 40 nm and array chip sizes of a few millimeters. This will be achieved by using the same material (silicon) for both the array chip and the medium substrate in conjunction with four integrated heat sensors that control four heaters on the chip to maintain a constant array-chip temperature during operation. True parallel operation of large 2D arrays results in very large chip sizes because of the space required for the individual write/read wiring to each cantilever and the many I/O pads. The row and column time-multiplexing addressing scheme implemented successfully in every DRAM is a very elegant solution to this issue. In the case of Millipede, the time-multiplexed addressing scheme is used to address the array row by row with full parallel write/read operation within one row.

The current Millipede storage approach is based on a new thermomechanical write/read process in nanometer-thick polymer films. As previously noted, thermomechanical writing in polycarbonate films and optical readback were first investigated and demonstrated with a single cantilever by Mamin and Rugar [2]. Although the storage density of 30 Gb/in.$^2$ obtained originally was not overwhelming, the results encouraged us to use polymer films as well to achieve density improvements.

## 3. Thermomechanical AFM data storage

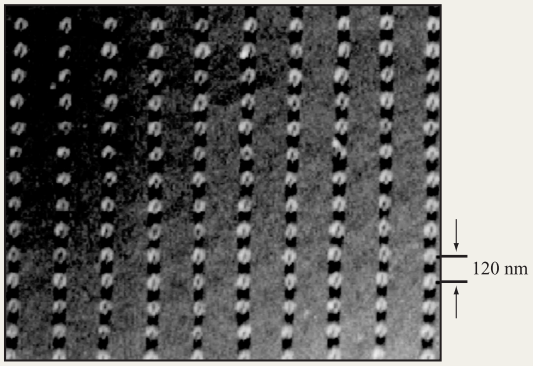
In recent years, AFM thermomechanical recording in polymer storage media has undergone extensive modifications, primarily with respect to the integration of sensors and heaters designed to enhance simplicity and to increase data rate and storage density. Using cantilevers with heaters, thermomechanical recording at 30 Gb/in.$^2$ storage density and data rates of a few Mb/s for reading and 100 Kb/s for writing have been demonstrated [2, 3, 11]. Thermomechanical writing is a combination of applying a local force by the cantilever/tip to the polymer layer and softening it by local heating. Initially, the heat transfer from the tip to the polymer through the small contact area is very poor, improving as the contact area increases. This means that the tip must be heated to a relatively high temperature (about 400°C) to initiate the melting process. Once melting has commenced, the tip is pressed into the polymer, which increases the heat transfer to the polymer, increases the volume of melted polymer, and hence increases the bit size. Our rough estimates indicate that at the beginning of the writing process only about 0.2% of the heating power is used in the very small contact zone (10–40 nm$^2$) to melt the polymer locally, whereas about 80% is lost through the cantilever legs to the chip body and about 20% is radiated from the heater platform through the air gap to the medium/substrate. After melting has started and the contact area has increased, the heating power available for generating the indentations increases by at least ten times to become 2% or more of the total heating power. With this highly nonlinear heat-transfer mechanism, it is very difficult to achieve small tip penetration and thus small bit sizes, as well as to control and reproduce the thermomechanical writing process.

This situation can be improved if the thermal conductivity of the substrate is increased, and if the depth of tip penetration is limited. We have explored the use of very thin polymer layers deposited on Si substrates to improve these characteristics [12, 13], as illustrated in **Figure 2**. The hard Si substrate prevents the tip from penetrating farther than the film thickness allows, and it enables more rapid transport of heat away from the heated region because Si is a much better conductor of heat than the polymer. We have coated Si substrates

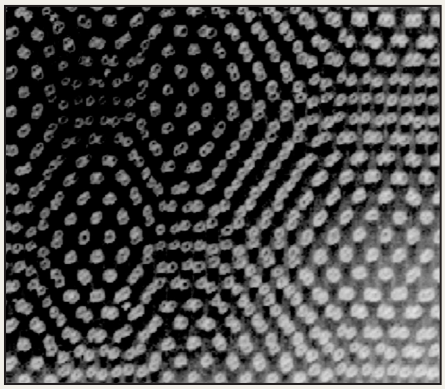
with a 40-nm film of polymethylmethacrylate (PMMA) and achieved bit sizes ranging between 10 and 50 nm. However, we noticed increased tip wear, probably caused by the contact between Si tip and Si substrate during writing. We therefore introduced a 70-nm layer of cross-linked photoresist (SU-8) between the Si substrate and the PMMA film to act as a softer penetration stop that avoids tip wear but remains thermally stable.

Using this layered storage medium, data bits 40 nm in diameter have been written, as shown in **Figure 3**. These results were obtained using a 1-$\mu$m-thick, 70-$\mu$m-long, two-legged Si cantilever [11]. The cantilever legs are made highly conducting by high-dose ion implantation, whereas the heater region remains low-doped. Electrical pulses 2 $\mu$s in duration were applied to the cantilever with a period of 50 $\mu$s. Figure 3(a) demonstrates that 40-nm bits can be written with 120-nm pitch, or very close to each other, without merging [Figure 3(b)], implying a potential bit areal density of 400 Gb/in.$^2$

Imaging and reading are done using a new thermomechanical sensing concept [14]. The heater cantilever originally used only for writing was given the additional function of a thermal readback sensor by exploiting its temperature-dependent resistance. The resistance ($R$) increases nonlinearly with heating power/temperature from room temperature to a peak value of 500–700°C. The peak temperature is determined by the doping concentration of the heater platform, which ranges from $1 \times 10^{17}$ to $2 \times 10^{18}$. Above the peak temperature, the resistance drops as the number of intrinsic carriers increases because of thermal excitation [15]. For sensing, the resistor is operated at about 350°C, a temperature that is not high enough to soften the polymer, as is necessary for writing. The principle of thermal sensing is based on the fact that the thermal conductance between the heater platform and the storage substrate changes according to the distance between them. The medium between a cantilever and the storage substrate—in our case air—transports heat from one side to the other. When the distance between heater and sample is reduced as the tip moves into a bit indentation, the heat transport through air will be more efficient, and the heater's temperature and hence its resistance will decrease. Thus, changes in temperature of the continuously heated resistor are monitored while the cantilever is scanned over data bits, providing a means of detecting the bits. **Figure 4** illustrates this concept. Under typical operating conditions, the sensitivity of thermomechanical sensing is even better than that of piezoresistive-strain sensing, which is not surprising because thermal effects in semiconductors are stronger than strain effects. The good $\Delta R/R$ sensitivity of about $10^{-5}$/nm is demonstrated by the images of the 40-nm-size bit indentations in Figure 3, which were obtained using the described thermal-sensing technique.




Pitch 120 nm
(a)



Variable pitch
(b)

Figure 3

Series of 40-nm data bits formed in a uniform array with (a) 120-nm pitch and (b) variable pitch (≥40 nm), resulting in bit areal densities of up to 400 Gb/in.$^2$ Images obtained with a thermal readback technique. Adapted from [12], with permission.

In addition to ultradense thermomechanical write/read, we have also demonstrated for the first time the erasing and rewriting capabilities of polymer storage media [12]. Thermal reflow of storage fields is achieved by heating the medium to about 150°C for a few seconds. The smoothness of the reflowed medium allowed multiple rewriting of the same storage field. This erasing process does not allow bit-level erasing; it will erase larger storage areas. However, in most applications single-bit erasing is not required anyway, because files or records are usually erased as a whole.

The erasing and multiple rewriting processes, as well as bit-stability investigations, are topics of ongoing research.

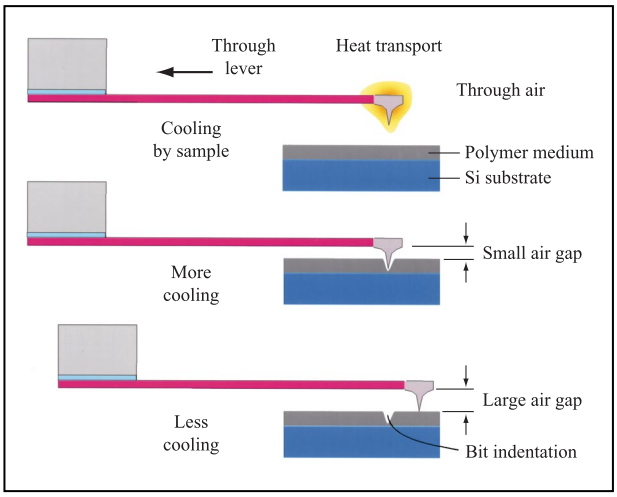



Figure 4

Principle of AFM thermal sensing. The heater cantilever is continuously heated by a dc power supply while it is being scanned and the heater resistivity measured. Adapted from [17(a)], with permission; © 1999 IEEE.

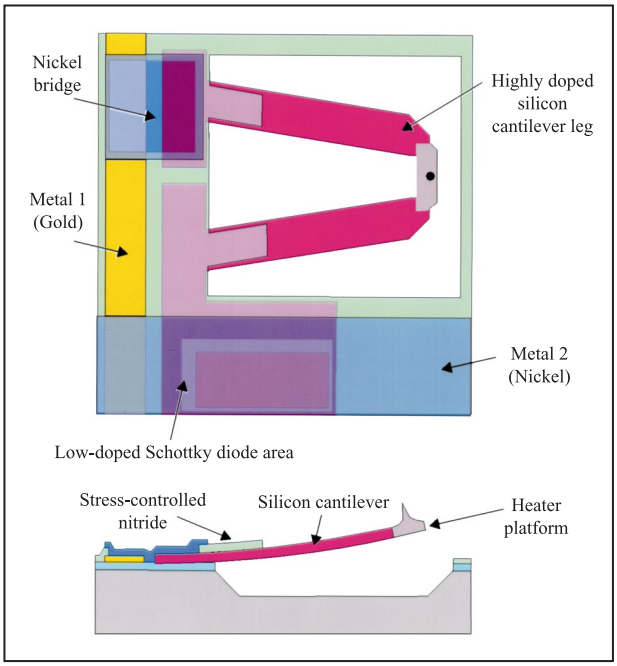



Figure 5

Layout and cross section of one cantilever cell. From [17(a)], reproduced with permission; © 1999 IEEE.

## 4. Array design, technology, and fabrication

As a first step, a 5 × 5 array chip was designed and fabricated to test the basic Millipede concept. All 25 cantilevers had integrated tip heating for thermomechanical writing and piezoresistive deflection sensing for read-back. No time-multiplexing addressing scheme was used for this test vehicle; rather, each cantilever was individually addressable for both thermomechanical writing and piezoresistive deflection sensing. A complete resistive bridge for integrated detection has also been incorporated for each cantilever.

The chip has been used to demonstrate *x*/*y*/*z* scanning and approaching of the entire array, as well as parallel operation for imaging. This was the first parallel imaging by a 2D AFM array chip with integrated piezoresistive deflection sensing. Details of the all-dry micromachining process for the fabrication of the 5 × 5 array and parallel imaging results are described in [10]. The imaging results also confirmed the global chip-approaching and -leveling scheme, since all 25 tips approached the medium within less than 1 $\mu$m of *z*-actuation. Unfortunately, the chip was not able to demonstrate parallel writing because of electromigration problems due to temperature and current density in the Al wiring of the heater. However, we learned from this 5 × 5 test vehicle that 1) global chip approaching and leveling is possible and promising, and 2) metal (Al) wiring on the cantilevers should be avoided to eliminate electromigration and cantilever deflection due to bimorph effects while heating.

Encouraged by the results of the 5 × 5 cantilever array, we designed and fabricated a 32 × 32 array chip. With the findings from the fabrication and operation of the 5 × 5 array and the very dense thermomechanical writing/reading in thin polymers with single cantilevers, we made some important changes in the chip functionality and fabrication processes. The major differences are 1) surface micromachining to form cantilevers at the wafer surface, 2) all-silicon cantilevers, 3) thermal instead of piezoresistive sensing, and 4) first- and second-level wiring with an insulating layer for a multiplexed row/column-addressing scheme.

Since the heater platform functions as a write/read element and no individual cantilever actuation is required, the basic array cantilever cell becomes a simple two-terminal device addressed by multiplexed *x*/*y* wiring, as shown in **Figure 5**. The cell area and *x*/*y* cantilever pitch is 92 $\mu$m × 92 $\mu$m, which results in a total array size of less than 3 mm × 3 mm for the 1024 cantilevers. The cantilever is fabricated entirely of silicon for good thermal and mechanical stability. It consists of the heater platform with the tip on top, the legs acting as a soft mechanical spring, and an electrical connection to the heater. They are highly doped to minimize interconnection resistance and replace the metal wiring on the cantilever to eliminate

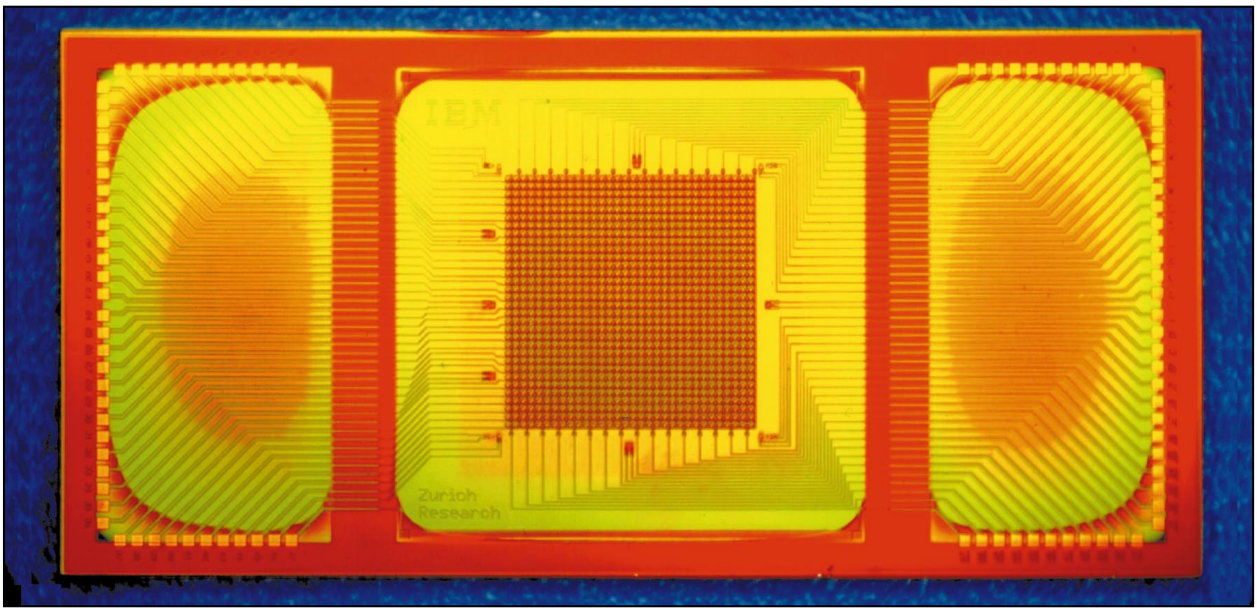



Figure 6

Photograph of fabricated chip (14 mm × 7 mm). The 32 × 32 cantilever array is located at the center, with bond pads distributed on either side. From [17(a)], reproduced with permission; © 1999 IEEE.

electromigration and parasitic *z*-actuation of the cantilever due to the bimorph effect. The resistive ratio between the heater and the silicon interconnection sections should be as high as possible; currently the highly doped interconnections are 400 Ω and the heater platform is 11 kΩ (at 4 V reading bias).

The cantilever mass must be minimized to obtain soft (flexible), high-resonant-frequency cantilevers. Soft cantilevers are required for a low loading force in order to eliminate or reduce tip and medium wear, whereas a high resonant frequency allows high-speed scanning. In addition, sufficiently wide cantilever legs are required for a small thermal time constant, which is partly determined by cooling via the cantilever legs [11]. These design considerations led to an array cantilever with 50-$\mu$m-long, 10-$\mu$m-wide, 0.5-$\mu$m-thick legs, and a 5-$\mu$m-wide, 10-$\mu$m-long, 0.5-$\mu$m-thick platform. Such a cantilever has a stiffness of 1 N/m and a resonant frequency of 200 kHz. The heater time constant is a few microseconds, which should allow a multiplexing rate of 100 kHz.

The tip height should be as small as possible because the heater platform sensitivity depends strongly on the distance between the platform and the medium. This contradicts the requirement of a large gap between the chip surface and the storage medium to ensure that only the tips, and not the chip surface, are making contact with the medium. Instead of making the tips longer, we purposely bent the cantilevers a few micrometers out of the chip plane by depositing a stress-controlled plasma-enhanced chemical vapor deposition (PECVD) silicon-nitride layer at the base of the cantilever (see Figure 5). This bending as well as the tip height must be well controlled in order to maintain an equal loading force for all cantilevers of an array.

Cantilevers are released from the crystalline Si substrate by surface micromachining using either plasma or wet chemical etching to form a cavity underneath the cantilever. Compared to a bulk-micromachined through-wafer cantilever-release process, as performed for our 5 × 5 array [10], the surface-micromachining technique allows an even higher array density and yields better mechanical chip stability and heat sinking. Because the Millipede tracks the entire array without individual lateral cantilever positioning, thermal expansion of the array chip must be either small or well-controlled. Because of thermal chip expansion, the lateral tip position must be controlled with better precision than the bit size, which requires array dimensions as small as possible and a well-controlled chip temperature. For a 3 mm × 3 mm silicon array area and 10-nm tip-position accuracy, the chip temperature has to be controlled to about 1°C. This is ensured by four temperature sensors in the corners of the array and heater

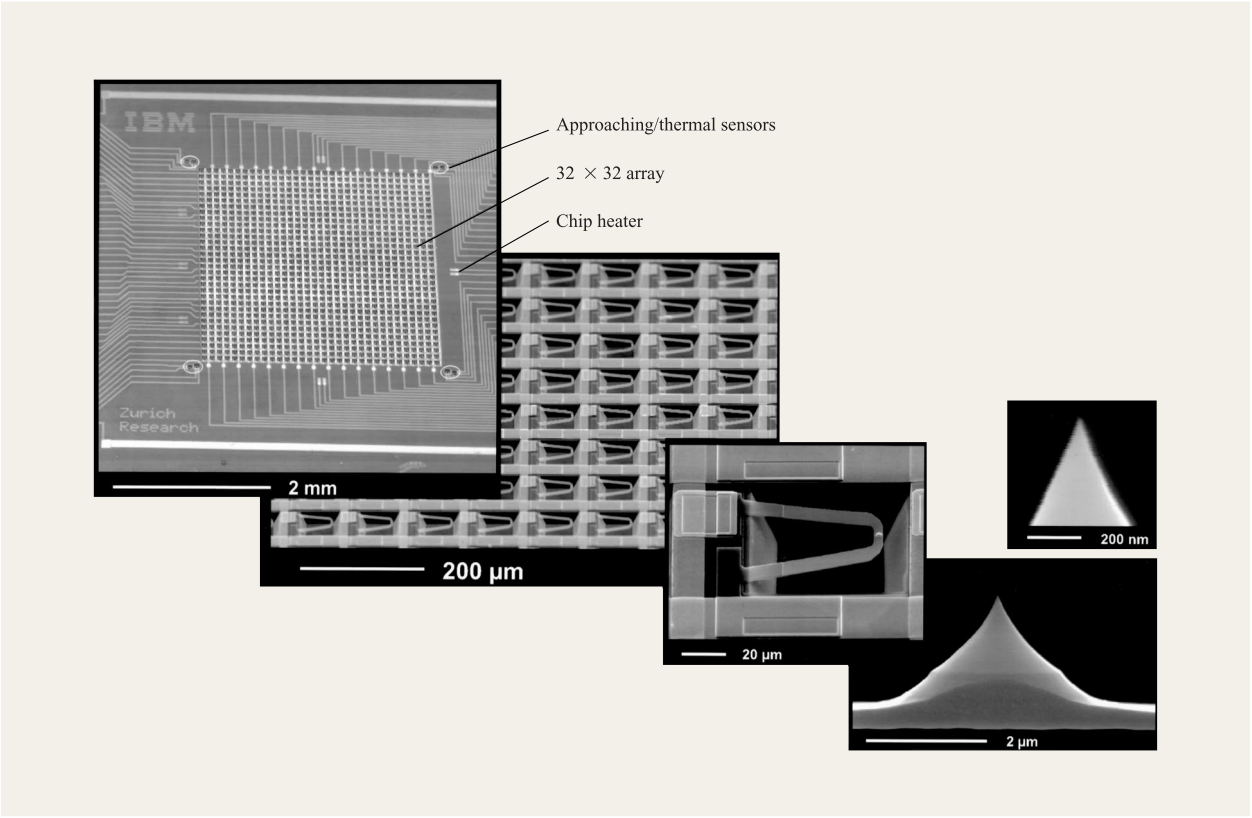



Figure 7

SEM images of the cantilever array section with approaching and thermal sensors in the corners, array and single cantilever details, and tip apex.

elements on each side of the array. Thermal expansion considerations were a strong argument for the 2D array arrangement instead of 1D, which would have made the chip 32 times longer for the same number of cantilevers.

The photograph in **Figure 6** shows a fabricated chip with the 32 × 32 array located in the center (3 mm × 3 mm) and the electrical wiring interconnecting the array with the bonding pads at the chip periphery.

**Figure 7** shows the 32 × 32 array section of the chip with the independent approach/heat sensors in the four corners and the heaters on each side of the array, as well as zoomed scanning electron micrographs (SEMs) of an array section, a single cantilever, and a tip apex. The tip height is 1.7 $\mu$m and the apex radius is smaller than 20 nm, which is achieved by oxidation sharpening [16].

The cantilevers are interconnected by integrating Schottky diodes in series with the cantilevers. The diode is operated in reverse bias (high resistance) if the cantilever is not addressed, thereby greatly reducing crosstalk between cantilevers. More details about the array fabrication are given in Reference [17].

## 5. Array characterization

The array's independent cantilevers, which are located in the four corners of the array and used for approaching and leveling of chip and storage medium, are used to initially characterize the interconnected array cantilevers. Additional cantilever test structures are distributed over the wafer; they are equivalent to but independent of the array cantilevers. **Figure 8** shows an $I/V$ curve of such a cantilever; note the nonlinearity of the resistance. In the low-power part of the curve, the resistance increases as a function of heating power, whereas in the high-power regime, it decreases.

In the low-power, low-temperature regime, silicon mobility is affected by phonon scattering, which depends on temperature, whereas at higher power the intrinsic temperature of the semiconductor is reached, resulting in a resistivity drop due to the increasing number of carriers [15]. Depending on the heater-platform doping concentration of $1 \times 10^{17}$ to $2 \times 10^{18}$ at./cm$^3$, our calculations estimate a resistance maximum at temperatures of 500°C and 700°C, respectively.

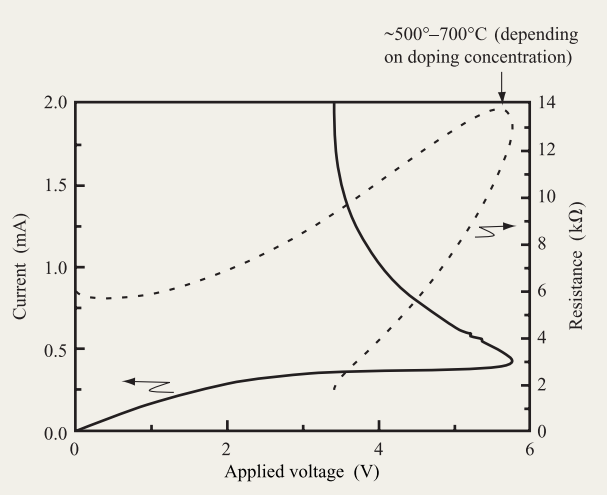



Figure 8

*I*/*V* curve of one cantilever. The curve is nonlinear owing to the heating of the platform as the power and temperature are increased. For doping concentrations between $1 \times 10^{17}$ and $2 \times 10^{18}$ at./cm$^3$, the maximum temperature varies between 500°C and 700°C. Reprinted from [17(b)], by permission of Elsevier Science.

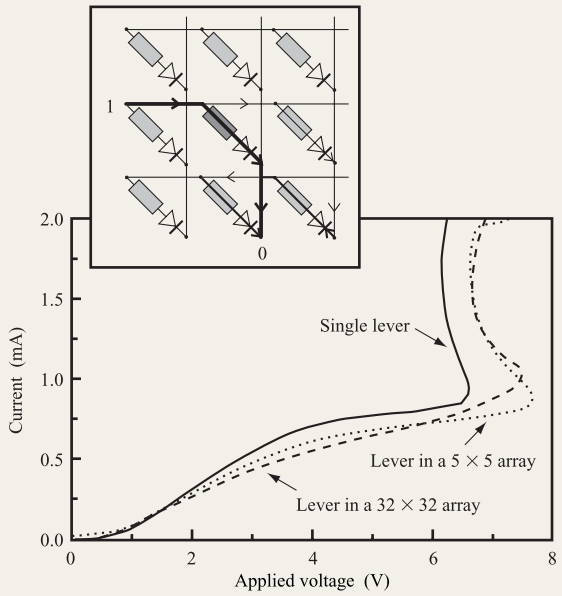



Figure 9

Comparison of the *I*/*V* curve of an independent cantilever (solid line) with the current response when addressing a cantilever in a 5 × 5 (dotted line) or a 32 × 32 (dashed line) array with a Schottky diode connected serially to the cantilever. Little change is observed in the *I*/*V* curve between the different cases. Also shown in the inset is a sketch representing the direct path (thick line) and a parasitical path (thin line) in a cantilever–diode array. In the parasitical path there is always one diode in reverse bias that reduces the parasitical current. Reprinted from [17(b)], by permission of Elsevier Science.

The cantilevers within the array are electrically isolated from one another by integrated Schottky diodes. Because every parasitic path in the array to the addressed cantilever of interest contains a reverse-biased diode, the crosstalk current is drastically reduced, as shown in **Figure 9**. Thus, the current response to an addressed cantilever in an array is nearly independent of the size of the array, as demonstrated by the *I*/*V* curves in Figure 9. Hence, the power applied to address a cantilever is not shunted by other cantilevers, and the reading sensitivity is not degraded—not even for very large arrays (32 × 32). The introduction of the electrical isolation using integrated Schottky diodes turned out to be crucial for the successful operation of interconnected cantilever arrays with a simple time-multiplexed addressing scheme. **Figure 10** shows the measured cantilever resistance uniformity across the array for both forward- and reverse-biased diodes. Good uniformity is essential for a robust write/read electronics design.

The tip-apex height uniformity within an array is very important because it determines the force of each cantilever while in contact with the medium and hence influences write/read performance as well as medium and tip wear. Wear investigations suggest that a tip-apex height uniformity across the chip of less than 500 nm is required [4], with the exact number depending on the spring constant of the cantilever. In the case of the Millipede, the tip-apex height is determined by the tip height and the cantilever bending. **Figure 11** shows the tip-apex height uniformity of one row of the array (32 tips) due to tip height and cantilever bending. It demonstrates that our uniformity is of the order of 100 nm, thus meeting requirements.

## 6. First write/read results with the 32 × 32 array chip

We have explored two *x*/*y*/*z* scanning approaching schemes to operate the array for writing/reading. The first one is based closely on the Millipede basic concept shown in Figure 1. A 3 mm × 3 mm silicon substrate is spin-coated with the SU-8/PMMA polymer medium structure described in Section 3. This storage medium is attached to a small magnetic *x*/*y*/*z* scanner and approaching device. The three magnetic *z*-approaching actuators bring the medium into contact with the tips of the array chip. The *z*-distance between the medium and the Millipede chip is controlled by the approaching sensors (additional

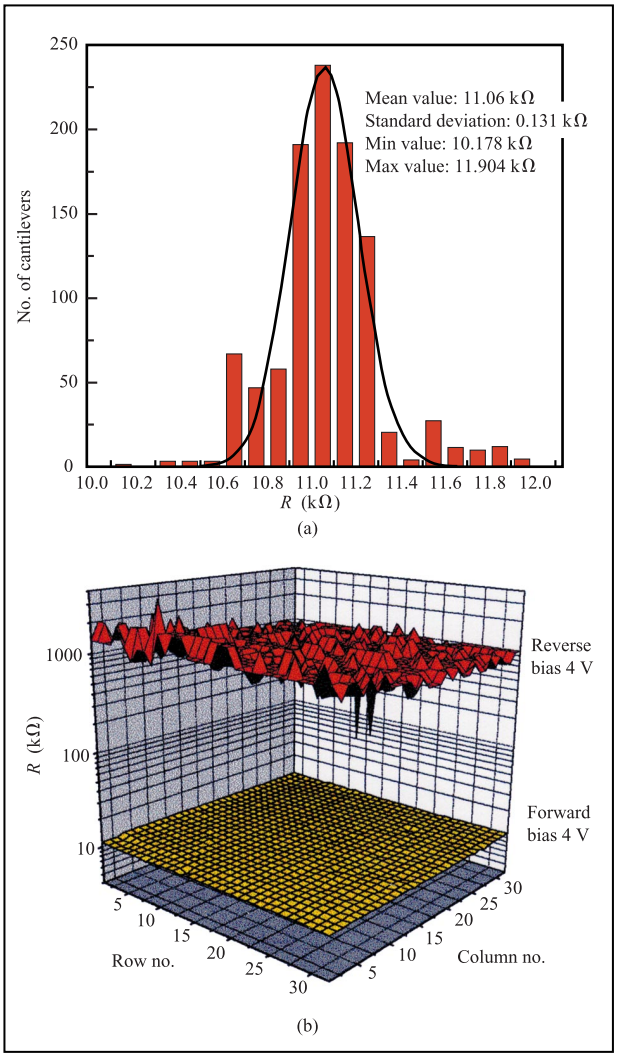



**Figure 10**

Cantilever resistance uniformity for forward- and reverse-biased diodes: (a) Resistance histogram (4 V forward bias); (b) resistance mapping in 4 V forward and reverse bias.

cantilevers) in the corners of the array. The signals from these cantilevers are used to determine the forces on the *z*-actuators and, hence, also the forces of the cantilever while it is in contact with the medium. This sensing and actuation feedback loop continues to operate during *x*/*y* scanning of the medium. The PC-controlled write/read scheme addresses the 32 cantilevers of one row in parallel. Writing is performed by connecting the addressed row for 20 $\mu$s to a high, negative voltage and simultaneously applying data inputs ("0" or "1") to the 32 column lines. The data input is a high, positive voltage for a "1" and ground for a "0." This row-enabling and column-addressing scheme supplies a heater current to all cantilevers, but only those cantilevers with high, positive voltage generate an indentation ("1"). Those with ground are not hot enough to make an indentation, and thus write a "0." When the scan stage has moved to the next bit position, the process is repeated, and this is continued until the line scan is finished. In the read process, the selected row line is connected to a moderate negative voltage, and the column lines are grounded via a protection resistor of about 10 kΩ, which keeps the cantilevers warm. During scanning, the voltages across the resistors are measured. If one of the cantilevers falls into a "1" indentation, it cools, thus changing the resistance and voltage across the series resistor. The written data bit is sensed in this manner.

The SEM and the AFM image in **Figure 12** show our first parallel writing/reading results. Figure 12(a) shows a SEM image of a large area of the polymer medium, in which the many small bright spots indicate the location of storage fields with data written by the corresponding cantilevers. The data written consisted of an IBM logo composed of indentations ("1"s) and clear separations ("0"s). Figure 12(b) shows magnified images of two storage fields. The dots are about 50 nm in diameter, which results in areal densities of 100–200 Gb/in.$^2$ depending on the ability to separate the bit indentations by a distinguishable amount. A first successful attempt demonstrates the read-back of the stored data by the integrated thermomechanical sensing: Figure 12(c) shows the raw read-back data of two different storage fields with areal density similar to that in 12(b). **Figure 13** is a photograph of the complete experimental Millipede setup.

The second *x*/*y*/*z* scanning and approaching system we explored, illustrated in **Figure 14(a)**, makes use of a modified magnetic hard-disk drive. The array chip replaced the magnetic write/read head slider and was mechanically leveled and fixed on the suspension arm. The *z*-approaching and -contacting procedure was performed by a piezoelectric actuator mounted on top of the suspension, which brought the array chip into contact with the medium and maintained it there. The 92-$\mu$m scanning in *x* was achieved by the standard voice-coil actuator of the suspension arm, whereas the *y*-scanning was performed by the slowly moving disk. The row/column-addressing scheme is very similar to the one used for the *x*/*y*/*z* scanner. The first writing results are shown by the SEM images in **Figures 14(b)** and **14(c)**. The bright lines in Figure 14(b) again identify the locations of the storage fields written by many cantilevers with 92-$\mu$m pitch in each direction, whereas Figure 14(c) shows the bit indentations of one storage field corresponding to 70–100 Gb/in.$^2$ This lower areal density is primarily due to the thicker PMMA layer (100 nm) used for this experiment. Reading operation is currently being investigated.

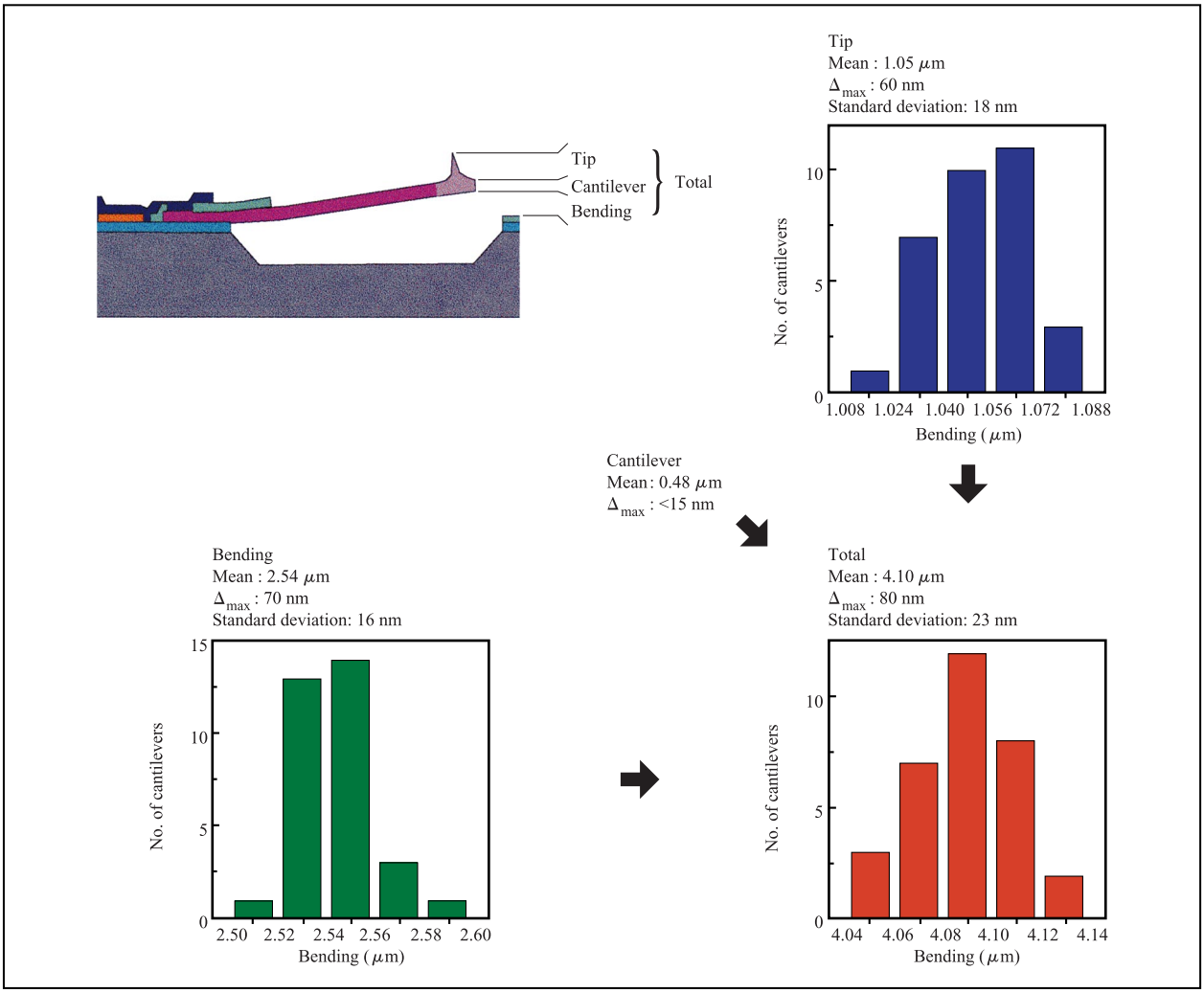



Figure 11

Tip-apex height uniformity across one cantilever row of the array, with individual contributions from the tip height and cantilever bending.

## 7. Discussion of possible Millipede applications in data storage

Our current 32 × 32 array chip is just one example of the many possible designs of a data-storage system; the design and concept depend strongly on the intended application. **Figure 15** shows the storage capacity and access time as a function of array size and cantilever pitch/scan range of a Millipede data-storage system according to the basic concept of Figure 1 assuming an areal density of 500 Gb/in.[2] It demonstrates the great potential for low- to high-end applications, of which the current 32 × 32 array is but one case. The two shaded circles in Figure 15 represent the storage capacity and access time for the current 32 × 32 array. It is important to note that the same data capacity can be achieved, for example, using large arrays with small cantilever pitch/scan range or, conversely, using small arrays with a larger scan range. In addition, terabit data capacity can be achieved by one large array, by many identical small ones operating in parallel, or by displacing a small array on a large medium. Out of this wide range of design and application scenarios, we would like to explain two cases of particular interest.

- *Small-form-factor storage system (Nanodrive)*

IBM's recent product announcement of the Microdrive represents a first successful step into miniaturized storage systems. As we enter the age of pervasive computing, we can assume that computer power is available virtually everywhere. Miniaturized and low-power storage systems will become crucial, particularly for mobile applications.

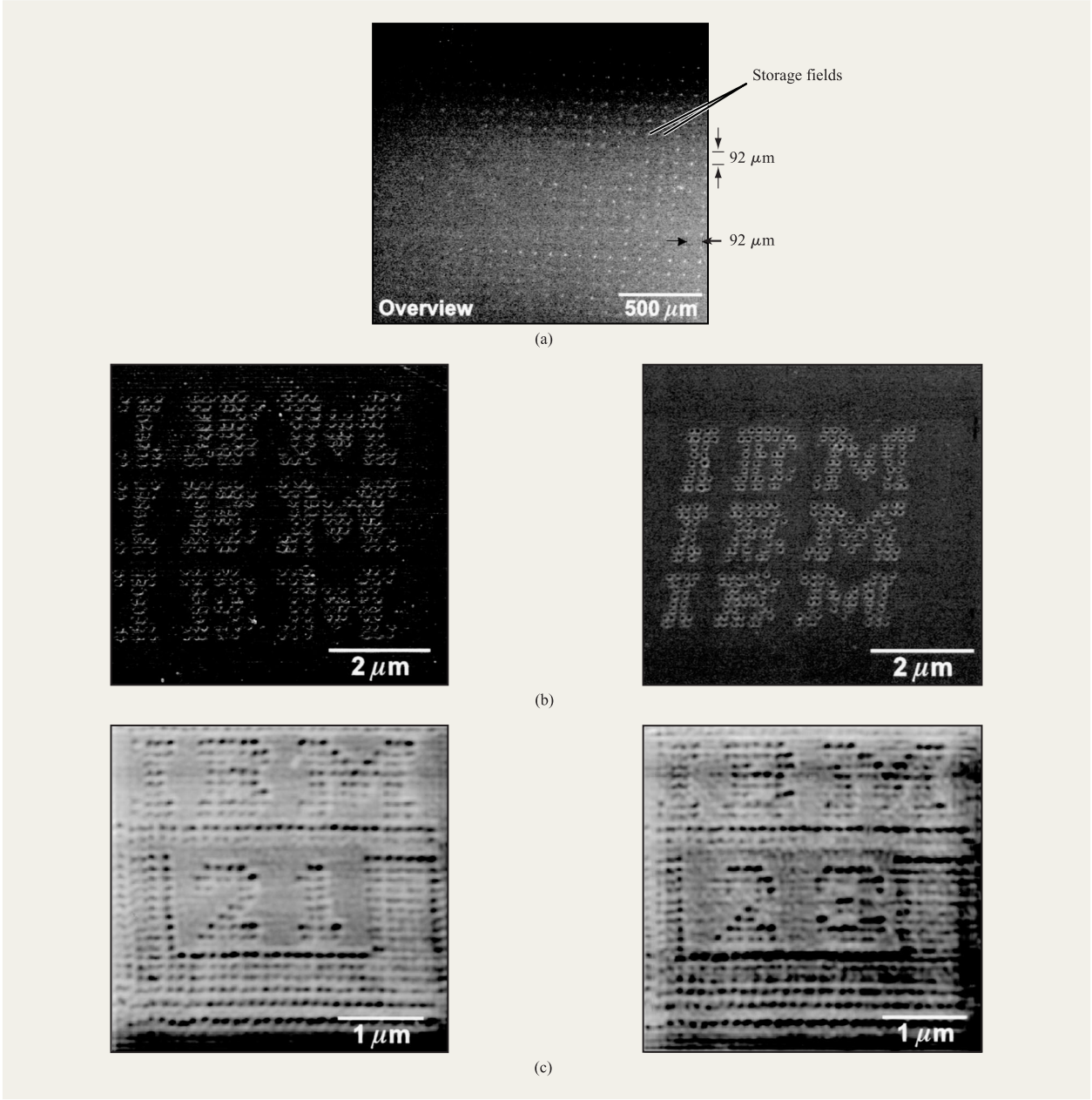



Figure 12

SEM images of *x*/*y*/*z* scanner Millipede writing results: (a) SEM image of many storage fields. (b) Magnified views of two individual storage fields with IBM logo represented by bit indentations/separations equivalent to a storage density of 100–200 Gb/in.$^2$ (50-nm-thick PMMA medium). (c) Thermomechanical read-back signals of two storage fields demonstrating areal density similar to those in (b).

The availability of storage devices with gigabyte capacity having a very small form factor (in the range of centimeters or even millimeters) will open up new possibilities to integrate such "Nanodrives" into watches, cellular telephones, laptops, etc., provided such devices have low power consumption.

We have recently demonstrated that the magnetic *x*/*y*/*z* scanner can be micromachined and miniaturized [18, 19] with potential for even further miniaturization. **Figure 16(a)** shows the basic principles of the integrated micromagnetic scanner concept, whereas **Figure 16(b)** is a photograph of the first micromachined silicon scanner.

Further details on the design and fabrication have been published in References [18, 19].

The array chip with integrated or hybrid electronics and the micromagnetic scanner are key elements demonstrated for a Millipede-based device called Nanodrive, which is of course also very interesting for audio and video consumer applications. All-silicon, batch fabrication, low-cost polymer media, and low power consumption make Millipede very attractive as a centimeter- or even millimeter-sized gigabyte storage system.

- *Terabit drive*

The potential for very high areal density renders the Millipede also very attractive for high-end terabit storage systems. As mentioned above, terabit capacity can be achieved with three Millipede-based approaches: 1) very large arrays, 2) many smaller arrays operating in parallel,

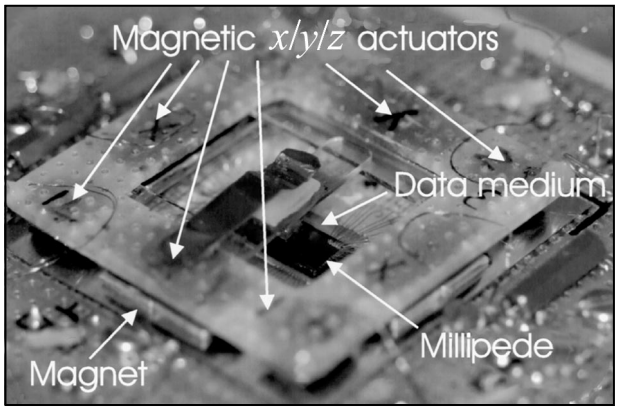



**Figure 13**

Photograph of experimental Millipede setup with *x*/*y*/*z* magnetic actuators.

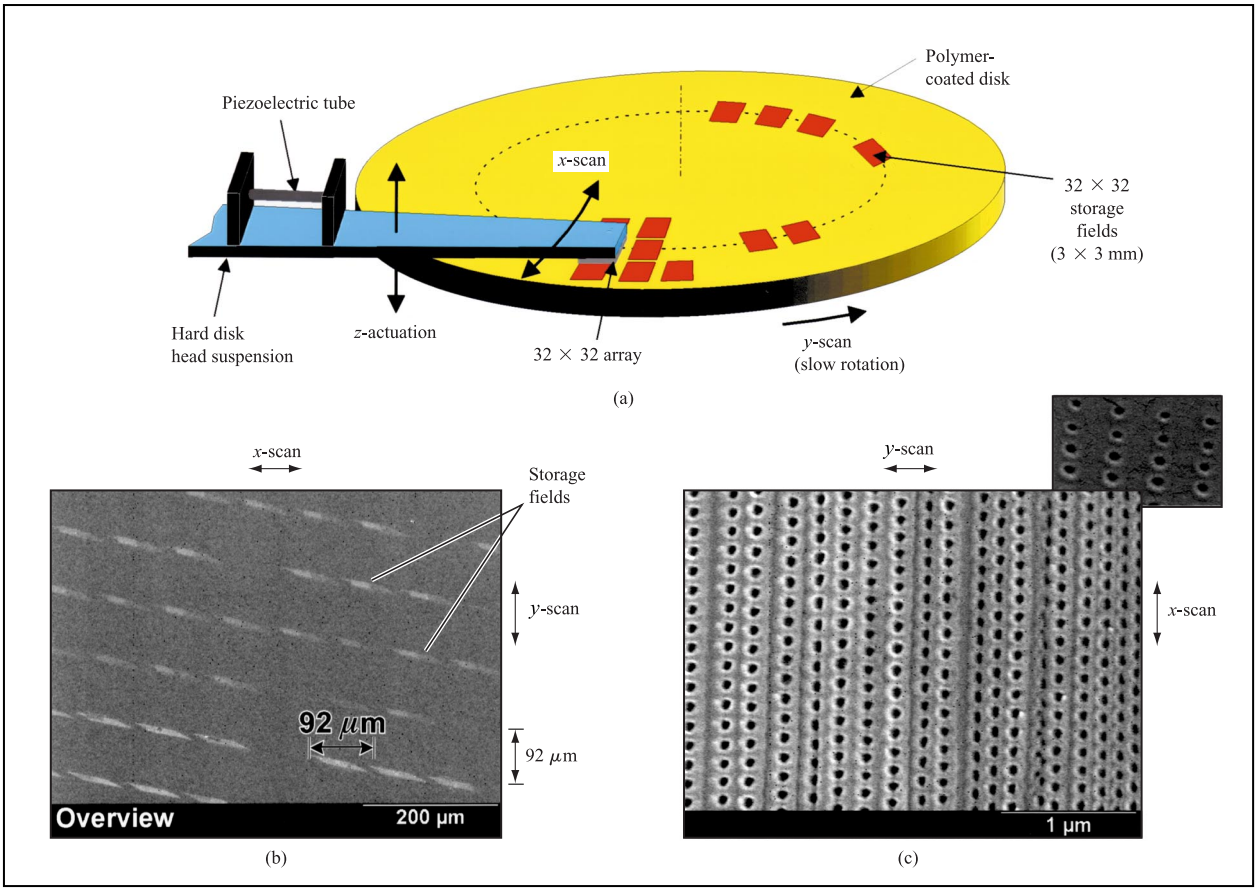



**Figure 14**

(a) Modified hard disk Millipede approach for array-chip scanning and displacement, and writing results: (b) SEM image of many storage fields; (c) magnified bit indentations in 100-nm-thick PMMA medium, equivalent to a storage density of 70–100 Gb/in.$^2$ Note that the *x*/*y* scan directions are interchanged between (b) and (c).

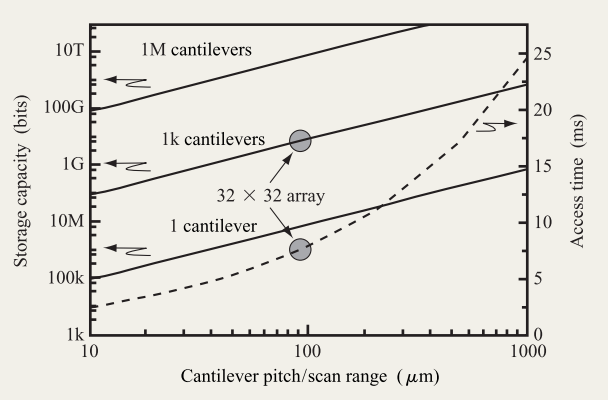



**Figure 15**

Storage capacity and access time vs. cantilever pitch/scan range for various array sizes, assuming 500-Gb/in.$^2$ storage density.

and 3) displacement of small/medium-sized arrays over large media.

Although the fabrication of considerably larger arrays ($10^5$ to $10^6$ cantilevers) appears to be possible, control of the thermal linear expansion will pose a considerable challenge as the array chip becomes significantly larger. The second approach is appealing because the storage system can be upgraded to fulfill application requirements in a modular fashion by operating many smaller Millipede units in parallel. The operation of the third approach was described above with the example of a modified hard disk. This approach combines the advantage of smaller arrays with the displacement of the entire array chip, as well as repositioning of the polymer-coated disk to a new storage location on the disk. A storage capacity of several terabits appears to be achievable on 2.5- and 3.5-in. disks. In addition, this approach is an interesting synergy of existing, reliable (hard-disk drive) and new (Millipede) technologies.

## 8. Summary and outlook

For the first time, we have fabricated and operated large 2D AFM arrays for thermomechanical data storage in thin polymer media. In doing so, we have demonstrated key milestones of the Millipede storage concept. The 400–500-Gb/in.$^2$ storage density we have demonstrated with single cantilevers is among the highest reported so far. The initial densities of 100–200 Gb/in.$^2$ achieved with the 32 × 32 array are very encouraging, with the potential of matching those of single cantilevers. Well-controlled processing techniques have been developed to fabricate array chips with good yield and uniformity. This VLSI–NEMS chip has the potential to open up new perspectives in many other applications of scanning probe techniques as well. Millipede is not limited to storage applications or polymer media. The concept is very general if the required functionality can be integrated on the cantilever/tip. This of course applies also to any other storage medium, including magnetic ones, making Millipede a possible universal parallel write/read head for future storage systems. Besides storage, other Millipede applications can be envisioned for large-area, high-speed imaging and high-throughput nanoscale

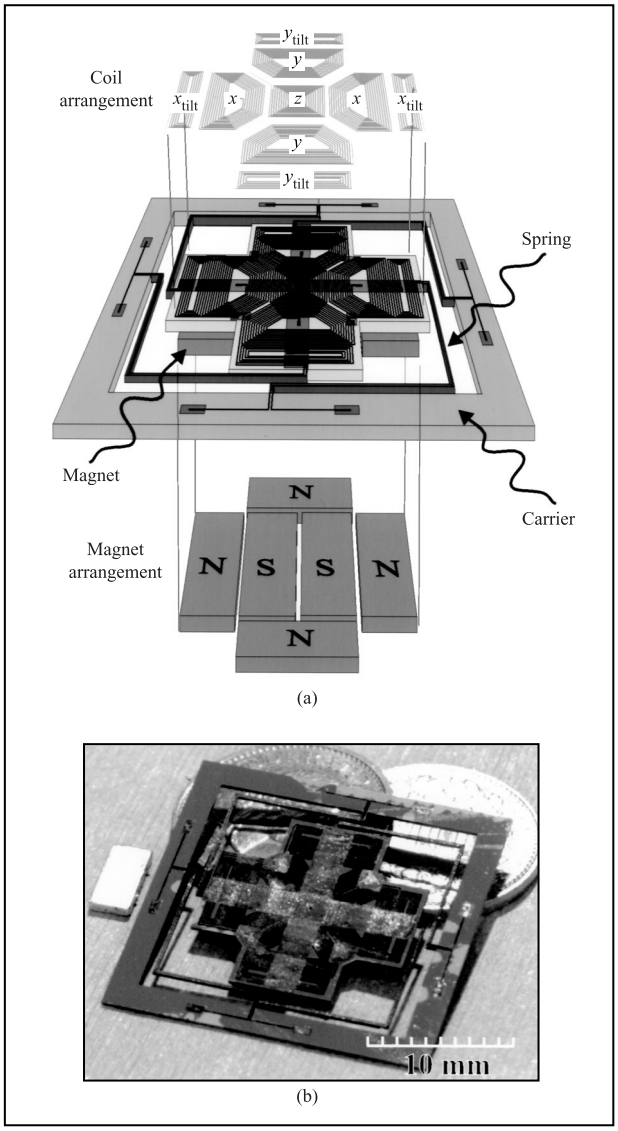



**Figure 16**

(a) Diagram illustrating basic concept of integrated micromagnetic $x/y/z$ scanner. (b) Photograph of micromachined $x/y/z$ scanner.

lithography [20, 21], as well as for atomic and molecular manipulation/modification.

The current Millipede array chip fabrication technique is compatible with CMOS circuits, which will allow future microelectronics integration. This is expected to produce better performance (speed) and smaller system form factors, as well as lower costs.

Although we have demonstrated the first high-density storage operations with the largest 2D AFM array chip ever built, a number of issues must be addressed before the Millipede can be considered for commercial applications; a few of these are listed below:

- Overall system reliability, including bit stability, tip and medium wear, erasing/rewriting.
- Limits of data rate (S/N ratio), areal density, array and cantilever size.
- CMOS integration.
- Optimization of write/read multiplexing scheme.
- Array-chip tracking.

Our near-term future activities are focused on these important aspects.

Finally, we would like to conclude with some thoughts and visions on the long-term outlook for the Millipede concept.

The highly parallel nanomechanical approach is novel in many respects. Recalling the transistor-to-microprocessor story mentioned at the beginning, we might ask whether a new device of a yet inconceivable level of novelty could possibly emerge from the Millipede. There is at least one feature of the Millipede that we have not yet exploited. With integrated Schottky diodes and the temperature-sensitive resistors on the current version of the Millipede array chip, we have already achieved the first and simplest level of micromechanical/electronic integration, but we are looking for much more complex ones to make sensing and actuation faster and more reliable. However, we envision something very much beyond this. Whenever there is parallel operation of functional units, there is the opportunity for sophisticated communication or logical interconnections between these units. The topology of such a network carries its own functionality and intelligence that goes beyond that of the individual devices. It could, for example, act as a processor. For the Millipede this could mean that a processor and VLSI–nanomechanical device may be merged to form a "smart" Millipede. We do not completely foresee what this could ultimately mean, but we do have a vision of the direction in which to go. If the Millipede is used, for example, as an imaging device, let us say for quality control in silicon chip fabrication, the amount of information it can generate is so huge that it is difficult to transmit these data to a computer to store and process them. Furthermore, most of the data are not of interest at all, so it would make sense if only the pertinent parts were predigested by the specialized smart Millipede and then transmitted. For this purpose, communication between the cantilevers is helpful because a certain local pattern detected by a single tip can mean something in one context and something else or even nothing in another context. The context might be derived from the patterns observed by other tips. A similar philosophy could apply to the Millipede as a storage device. A smart Millipede could possibly find useful pieces of information very quickly by a built-in complex pattern recognition ability, e.g., by ignoring information when certain bit patterns occur within the array. The bit patterns are recognized instantaneously by logical interconnections of the cantilevers. Even with this somewhat vague vision, we are very confident that the "smart" Millipede will have interesting long-term prospects in many application fields, possibly in fields that we cannot even envision today.

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## References

1. E. Grochowski and R. F. Hoyt, "Future Trends in Hard Disk Drives," *IEEE Trans. Magn.* **32,** 1850–1854 (1996).
2. H. J. Mamin and D. Rugar, "Thermomechanical Writing with an Atomic Force Microscope Tip," *Appl. Phys. Lett.* **61,** 1003–1005 (1992).
3. R. P. Ried, H. J. Mamin, B. D. Terris, L. S. Fan, and D. Rugar, "6-MHz 2-N/m Piezoresistive Atomic-Force-Microscope Cantilevers with Incisive Tips," *J. Microelectromech. Syst.* **6,** 294–302 (1997).
4. B. D. Terris, S. A. Rishton, H. J. Mamin, R. P. Ried, and D. Rugar, "Atomic Force Microscope-Based Data Storage: Track Servo and Wear Study," *Appl. Phys. A* **66,** S809–S813 (1998).
5. H. J. Mamin, B. D. Terris, L. S. Fan, S. Hoen, R. C. Barrett, and D. Rugar, "High-Density Data Storage Using Proximal Probe Techniques," *IBM J. Res. Develop.* **39,** 681–700 (1995).
6. H. J. Mamin, R. P. Ried, B. D. Terris, and D. Rugar, "High-Density Data Storage Based on the Atomic Force Microscope," *Proc. IEEE* **87,** 1014–1027 (1999).
7. D. A. Thompson and J. S. Best, "The Future of Magnetic Data Storage Technology," *IBM J. Res. Develop.* **44,** 311–322 (2000, this issue).

8. G. K. Binnig, H. Rohrer, and P. Vettiger, "Mass-Storage Applications of Local Probe Arrays," U.S. Patent 5,835,477, November 10, 1998.
9. P. Vettiger, J. Brugger, M. Despont, U. Drechsler, U. Dürig, W. Häberle, M. Lutwyche, H. Rothuizen, R. Stutz, R. Widmer, and G. Binnig, "Ultrahigh Density, High-Data-Rate NEMS-Based AFM Data Storage System," *J. Microelectron. Eng.* **46,** 11–17 (1999).
10. M. Lutwyche, C. Andreoli, G. Binnig, J. Brugger, U. Drechsler, W. Häberle, H. Rohrer, H. Rothuizen, and P. Vettiger, "Microfabrication and Parallel Operation of $5 \times 5$ 2D AFM Cantilever Array for Data Storage and Imaging," *Proceedings of the IEEE 11th International Workshop on Micro Electro Mechanical Systems* (*MEMS '98*), Heidelberg, Germany, January 1998, pp. 8–11; M. Lutwyche, C. Andreoli, G. Binnig, J. Brugger, U. Drechsler, W. Häberle, H. Rohrer, H. Rothuizen, P. Vettiger, G. Yaraliglu, and C. Quate, "$5 \times 5$ 2D AFM Cantilever Arrays: A First Step Towards a Terabit Storage Device," *Sensors & Actuators A* **73,** 89–94 (1999).
11. B. W. Chui, H. J. Mamin, B. D. Terris, D. Rugar, K. E. Goodson, and T. W. Kenny, "Micromachined Heaters with 1-$\mu$s Thermal Time Constants for AFM Thermomechanical Data Storage," *Proceedings of IEEE Transducers '97*, Chicago, June 1997, pp. 1085–1088.
12. G. Binnig, M. Despont, U. Drechsler, W. Häberle, M. Lutwyche, P. Vettiger, H. J. Mamin, B. W. Chui, and T. W. Kenny, "Ultra High-Density AFM Data Storage with Erase Capability," *Appl. Phys. Lett.* **74,** 1329–1331 (1999).
13. G. K. Binnig, M. Despont, W. Häberle, and P. Vettiger, "Method of Forming Ultrasmall Structures and Apparatus Therefor," filed at the U.S. Patent Office, March 17, 1999, Application No. 147865.
14. G. K. Binnig, J. Brugger, W. Häberle, and P. Vettiger, "Investigation and/or Manipulation Device," filed at the U.S. Patent Office, March 17, 1999, Application No. 147867.
15. S. M. Sze, *Physics of Semiconductor Devices*, John Wiley, New York, 1981.
16. T. S. Ravi and R. B. Marcus, "Oxidation Sharpening of Silicon Tips," *J. Vac. Sci. Technol. B* **9,** 2733–2737 (1991).
17. (a) M. Despont, J. Brugger, U. Drechsler, U. Dürig, W. Häberle, M. Lutwyche, H. Rothuizen, R. Stutz, R. Widmer, G. Binnig, H. Rohrer, and P. Vettiger, "VLSI–NEMS Chip for AFM Data Storage," *Technical Digest, 12th IEEE International Micro Electro Mechanical Systems Conference* (*MEMS'99*), Orlando, FL, January 1999, pp. 564–569; (b) *idem*, "VLSI–NEMS Chip for Parallel AFM Data Storage," *Sensors & Actuators A* (1999, in press).
18. M. Lutwyche, U. Drechsler, W. Häberle, R. Widmer, H. Rothuizen, P. Vettiger, and J. Thaysen, "Planar Micromagnetic *x*/*y*/*z* Scanner with Five Degrees of Freedom," *Magnetic Materials, Processes, and Devices: Applications to Storage and Microelectromechanical Systems* (*MEMS*), L. T. Romankiw, S. Krongelb, and C. H. Ahn, Eds., Vol. **98-20,** The Electrochemical Society, Pennington, NJ, 1999, pp. 423–433.
19. H. Rothuizen, U. Drechsler, G. Genolet, W. Häberle, M. Lutwyche, R. Stutz, R. Widmer, and P. Vettiger, "Fabrication of a Micromachined Magnetic *x*/*y*/*z* Scanner for Parallel Scanning Probe Applications," *Proceedings of the International Conference on Micro- and Nano-Engineering* (*MNE '99*), Rome, Italy, September 21–23, 1999, *Microelectron. Eng.* (in press).
20. S. C. Minne, G. Yaralioglu, S. R. Manalis, J. D. Adams, A. Atalar, and C. F. Quate, "Automated Parallel High-Speed Atomic Force Microscopy," *Appl. Phys. Lett.* **72,** 2340–2342 (1998).
21. N. C. MacDonald, "Nanomechanisms and Tips for Microinstruments," *Digest of Technical Papers*, *7th International Conference on Solid-State Sensors and Actuators*, Yokohama, Japan, June 7–10, 1993, pp. 8–12.

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